The IDC Engineers

Pocket Guide

Fifth Edition - Electronics

Personal Computers
Digital Signal Processing and
Analog/Digital Conversions

IDC TECHNOLOGIES

Technology Training that Works

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Foreword

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The objective of this booklet is to provide today's engineer with useful technical information and as an aide-memoir when you need to refresh your memory. This 5th edition of the Pocket Guide Series has been updated to include new information including Personal Computing and Digital Signal Processing.

Concepts that are important and useful to the engineer, scientist and technician, independent of discipline, are covered in this useful booklet.

Although IDC Technologies was founded in Western Australia in 1986, it now draws engineers from all countries. IDC Technologies currently has offices in Australia, Canada, Ireland, Malaysia, New Zealand, Singapore, South Africa, UK and USA.

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Notes

Chapter 1
The Personal Computer

The original Personal Computer (PC) was introduced by IBM in September 1981. Since then many different models have been developed and marketed by IBM and by many other manufacturers.

This chapter discusses the most important features of the PC and in particular how they relate to engineers, technicians and scientists.

There are five main types of microprocessors found in PCs. These are the 8088/8086, 80286, 80386, 80486 and the Pentium, all originally designed and sourced by Intel.

8086 Segmented Memory Architecture

All the various PC microprocessors have their origin in the Intel 8086 microprocessor. This is a 16-bit processor with a 16-bit data bus and 20-bit address space, which allows 2^{20} = 1,048,576 bytes or 1 MB of memory to be accessed.

The address registers of the 8086 are 16 bits wide and can only address 64 KB of memory. To obtain the real address of a memory location, the CPU adds the offset, contained in a CPU register, to the contents of a 16-bit segment register that has been shifted four bits to the left, to provide for the extra four address lines. Thus, the processor accesses memory in 64 KB segments, with the position of the segments in the address range controlled by the four segment registers.

This confusing and inefficient addressing scheme was inherited because of a need to maintain compatibility with earlier generations of processors. More recent processors, that is from the 80386 onwards, use full 32-bit addressing.

System Components

A few of the system components that are contained in a typical PC are discussed below. These are:

- memory and memory expansion
- display systems
- Industry Standard Architecture (ISA) bus

A brief discussion is then given of:

- polled data transfer
- ISA interrupts
- ISA DMA

Memory and Memory Expansion

There are three main classifications of memory used in PC systems. These are:

- base memory
- expanded memory
- extended memory

Base Memory

The memory from address 0 up to either the amount of memory installed in the computer or address FFFFFh (that is, up to a total of 1 MB) is called base memory. The first 640 KB of this is RAM and is normally used by the operating system and application programs. The remaining 384 KB of address space is reserved for the BIOS ROM and other adaptor ROMs, display adaptor memory, other adaptor memory and expanded memory.

Expanded Memory System (EMS)

Early processors (the 8086/8088), and all other PC processors running in real mode, are limited to a memory space of 1 MB because only the first 20 address lines are available. The same is true for DOS, being a 16-bit operating system. To make more memory available for applications, a scheme was developed by Lotus, Intel and Microsoft called Expanded Memory of which LIM EMS 4.0 is a common version.

In hardware, a second linear array of memory, called the logical expanded memory, is designed into a system. This can be up to 32 MB in size. A block of memory space is then set aside in the high memory area (normally 64 KB) and divided into four separate 16 KB pages. This acts as a window into the expanded memory. Thus, four pages of the actual expanded memory are accessible at any one time through the window in high memory. These windows are called page frames. The required portion of expanded memory is mapped into the page frame through registers in the computer's I/O space. Figure 1.1 illustrates the concept.

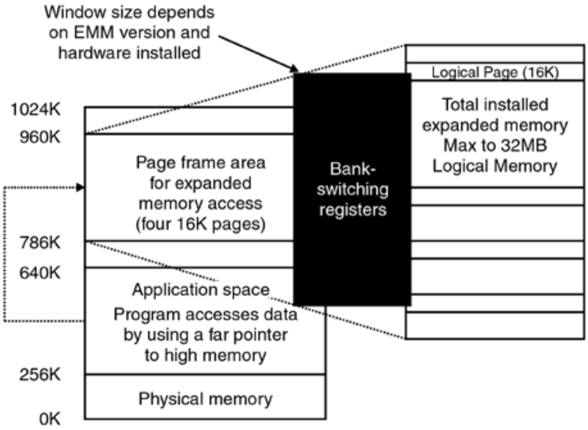


Figure 1.1
Organisation of Expanded Memory

The management of the memory is handled by the Expanded Memory Manager (EMM) which is an operating system extension normally installed at system startup. Application programs use the expanded memory for data. It is not usually possible to place program code in EMS. The application program communicates with the EMM via software interrupt 67h and accesses the memory via a far pointer into the page frame.

Extended Memory (XMS)

Extended memory is the physical linear memory found above the 1 MB mark. 80286 and 80386SX processors can address up to 16 MB of base and XMS while 80386DX and 80486 processors can address up to 4 GB of this type of memory. XMS is memory addressed directly by the processor (and hence the application program) and is therefore simpler, quicker and more efficient. Extended memory is only available as normal application memory when the processor is in protected mode; it follows that only 32-bit protected mode systems and extensions — such as OS/2, UNIX and MS-Windows but not DOS — can make this memory available to programs.

Display Systems

The 1024 x 768 Extended VGA is the de-facto standard for PC systems today. VGA adaptor boards have several programmable components, including a CRT controller, a sequencer, an attribute controller and a graphics contoller. The VGA ROM BIOS on the board contains a set of routines that perform screen I/O and display configuration. These routines, callable through interrupt 10 h, include functions to:

- set the video mode
- control the position and shape of the cursor
- read and write characters to the screen
- set the color palette
- read and write individual pixels
- obtain status information

The display may be configured into various modes which are different in the following ways:

- vertical resolution
- horizontal resolution
- data representation in the video buffer memory
- attribute decoding (colors, blinking and intensity)

The screen image is completely refreshed between 43.5 and 70 times per second, depending on the video mode. As each line of pixels is displayed the red, green and blue signals produced by the VGA board modulate the intensity of the electron beam. The scan cycle begins with the first pixel of the displayed video buffer data near the top left of the screen. The monitor moves the beam from left to right at a constant rate across each scan line and downward from scan line to scan line.

The VGA board produces a horizontal synchronization (or sync) signal that controls the timing of the deflection of the beam from the right hand end of the previous scan line to the start of the next scan line. The deflection is called the horizontal retrace.

The VGA board also produces a vertical synchronisation signal that controls the deflection of the beam from the end of the bottom scan line back to the top left of the screen. This is called the vertical retrace.

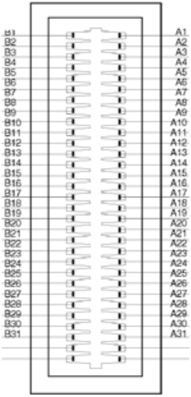
Industry Standard Architecture (ISA) Bus

The ISA bus signals are divided into four groups according to their function:

- address and data bus signal group
- data transfer control signal group
- bus arbitration signal group
- utility signal group

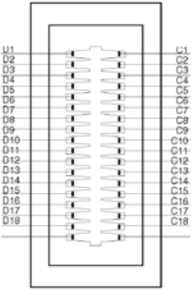
Facing rear panel with mounting brackets

I/O PIN	SIGNAL NAME	I/O
B1	GND	GROUND
B2	RESDRV	O
B3	+5 Vdc	POWER
B4	IRQ 9	I
B5	- 5 Vdc	POWER
B6	DRQ2	I
B7	- 12 Vdc	POWER
B8	NOWS	I
B9	+ 12 Vdc	POWER
B10	GND	GROUND
B11	/SMWTC	O
B12	/SMRDC	O
B13	/IOWC	I/O
B14	/IORC	I/O
B15	/DAK3	O
B16	DRQ3	I
B17	/DAK1	O
B18	DRQ1	I
B19	/REFRESH	I/O
B20	BCLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	/DAK2	O
B27	T-C	O
B28	BALE	O
B29	+ 5 Vdc	POWER
B30	OSC	O
B31	GND	GROUND



I/O PIN	SIGNAL NAME	I/O
A1	/IOCHK	I
A2	D7	I/O
A3	D6	I/O
A4	D5	I/O
A5	D4	I/O
A6	D3	I/O
A7	D2	I/O
A8	D1	I/O
A9	D0	I/O
A10	CHRDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O PIN	SIGNAL NAME	I/O
D1	/M16	I
D2	/IO16	I
D3	IRQ 10	I
D4	IRQ 11	I
D5	IRQ 12	I
D6	IRQ 15	I
D7	IRQ 14	I
D8	/DAKO	O
D9	DRQO	I
D10	/DAK5	O
D11	DRQ5	I
D12	/DAK6	O
D13	DRQ6	I
D14	/DAK7	O
D15	DRQ7	I
D16	+5 Vdc	POWER
D17	/MASTERIG	I
D18	GND	GROUND



I/O PIN	SIGNAL NAME	I/O
C1	/SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	/MRDC	I/O
C10	/MWTC	I/O
C11	D8	I/O
C12	D9	I/O
C13	D10	I/O
C14	D11	I/O
C15	D12	I/O
C16	D13	I/O
C17	D14	I/O
C18	D15	I/O

Facing front of computer

Figure 1.2
ISA Signal Mnemonics, Signal Directions and Pin Locations

Address and Data Bus Signal Group

This group contains the signal lines that are used to address memory and I/O devices and the signal lines used to transfer the actual data.

- D[7..0]

  D[7..0] are the low eight bits of the 16-bit bidirectional data bus used to transmit data between the microprocessor, memory and I/O port.

- D[15..8]

  D[15..] are the high eight bits of the 16-bit bidirectional data bus. They are similar to the lower eight data lines, D[7..0].

- LA[23..17]

  The LA17 to LA23 (latchable address) lines form part of the latchable address bus.

- SA[19..0]

  Address lines SA0 through SA19 are used to address system bus I/0 and memory devices. They form the lower-order 20 bits of the 32-bit address bus (however, only 24 of the 32 address lines are normally available in ISA systems).

- /SBHE

  /SBHE (System Bus High Enable) is an output-only signal. When low, it indicates to the expansion board that the present cycle expects to transfer data on the high half of the D[15..0] data bus.

- AEN

  When low, AEN (Address Enable) indicates that an I/O slave may respond to addresses and I/O commands on the bus.

Data Transfer Control Signal Group

This group contains signals that are used to control data transfer cycles on the bus.

- BCLK

  BCLK (Bus Clock) is provided to synchronise events with the main system clock.

- BALE

  When high, BALE (Address Latch Enable) indicates that a valid address is present on the latchable address lines LA17 to LA23. It goes high before the addresses are valid and falls low after they have become valid.

- /MRDC

  This signal is asserted by the system board or ISA bus master to indicate that the addressed memory slave should drive its data onto the system data bus.

- /SMRDC

  This memory-read signal is derived from /MRDC and has similar timing, the difference between the two is that /SMRDC is only active for addresses between Oh and 000FFFFFh (that is, in the first megabyte of memory).

- /MWTC

  This signal is asserted by the system board or ISA bus master to indicate that the addressed memory slave may latch data from the system data bus.

- /SMWTC

  This memory-write signal is derived from /MWTC and has similar timing; the difference between the two is that /SMWTC is only active for addresses between Oh and 000FFFFFh (that is, in the first megabyte of memory).

- /IORC

  The I/0-read signal is asserted by the system board or ISA bus master to indicate that the addressed I/0 slave should drive its data onto the system data bus.

- CHRDY

  An expansion device may use CHRDY (CHannel ReaDY) to lengthen a bus cycle from the default time.

- /NOWS

  The /NOWS (NO Wait State) signal may be driven by a memory device after it has decoded its address and command to indicate that the remaining BCLK periods in the present cycle are not required.

- /M16

  If the addressed memory is capable of transferring 16-bits of data at once on the D[15..0] datalines, it may assert /M16, after decoding a valid address.

- /1016

  If the addressed I/0 port is capable of transferring 16-bits of data at once on the D[15..0] datalines, it may assert /IO16, after decoding a valid address.

Bus Arbitration Signal Group

These signals are used to arbitrate between devices and the system board for control of the bus.

- DRQ[7..5] and DRQ[3..0]

  The DRQ (DMA request) lines are used to request a DMA service from the DMA subsystem, or for a 16-bit ISA bus master to request access to the system bus. The request is made when the DRQ line is driven high and may be asserted asynchronously.

- T-C

  T-C (Terminal Count) is a bidirectional signal acting in one of two modes, depending on the programming of the DMA channel. In output mode, the system board asserts T-C to indicate that a DMA channel's word count has reached its terminal value.

- /MASTER16

  This signal allows bus master cards to take over the system bus. A master asserts /MASTER16 when it receives a /DAK signal from a DRQ on its DMA channel.

- /REFRESH

  When low, /REFRESH indicates that a refresh cycle is in progress. This causes SA[15..0], or LA[15..2], to drive the row address inputs of all DRAM banks so that when /MRDC is asserted, the entire system memory is refreshed at one time.

Utility Signal Group

- OSC

  OSC is a clock signal for use in general timing applications. Its frequency is 14.31818 Mhz (roughly 70 ms) with a duty cycle of 50%.

- RESDRV

  RESDRV (reset driver) is an output signal which, when asserted, produces a hardware reset for devices attached to the bus.

- IRQ[15..14]
- IRQ[12..9]
- IRQ[7..3]

  The input-only interrupt lines are used by expansion boards to interrupt the CPU to request some service.

- /IOCHK

  An expansion board can assert /IOCHK (I/0 channel check) to indicate that a serious error has occurred.

Polled Data Transfer

The term polled data transfer refers to the transfer of data, to or from the CPU, that are initiated by a CPU instruction. These are memory and I/O reads and writes.

There are two sizes of data transfer: 8-bit and 16-bit, each with its own default timing. For backward compatibility with 8-bit devices, if a 16-bit instruction is executed by the CPU and the expansion board does not indicate that it is a 16-bit device (with either the /M16 or /IO16 signals), then the system board performs data bus translations. The 16-bit operation is converted into two 8-bit operations, and two 8-bit cycles are run instead of a single 16-bit cycle.

The 80286, 80386 and 80486 processors have a machine cycle consisting of two clock periods or states. These are called TS, send status and TC, perform command. The processor machine cycle may be extended by additional command (TC) states when the processor is in the command state by driving its /READY input. This is achieved on the ISA bus with the CHRDY signal, and the additional TC states are called wait states.

Wait states are added by the system board to ensure compatible timing. They may also be added and reduced by expansion boards. As BCLK, the I/O clock, is generally slower than the CPU clock, the system board lengthens the periods of the machine states in machine cycles that are to be run on the I/O bus. For example, if the CPU clock is 40 Mhz and the I/O clock is 10 Mhz, each T state in an I/O cycle will be lengthened by a factor of four over that of the main CPU.

ISA Interrupts

Interrupts provide the computer with a means of attending to important events on demand when they occur. Examples of such events are key strokes and COM port data. Interrupts allow the CPU to execute the main program and process only I/O data when it is available, instead of having to poll the I/O devices regularly, just in case there might be data available or a service to perform. This makes better use of CPU time, and is highly effective for fairly low-speed data transfer or event reaction (20 to 40 kHz max on a 40 MHz 386).

An interrupt is not an expansion bus cycle but a cycle on the computer system board, as noted above. The only hardware signalling, an adaptor performs to request an interrupt service from the CPU, is to drive its interrupt line from the low to the high state and keep it there until the interrupt is serviced. Any actual data transfer cycles are carried out by the software, using the CPU as discussed in the previous section on polled data transfer. The software data transfer is initiated by an interrupt signal.

There are three groups of interrupts that can occur in a PC system:

- Hardware Interrupts - where a device asserts its interrupt line
- Software Interrupts - generated when the CPU executes an interrupt instruction in program code
- Processor Exceptions - generated when an illegal operation is performed in the software (for example division by zero)

Interrupts all function in the same way. The first 1 KB of system memory is reserved for what are called interrupt vectors. An interrupt vector is a memory location (actually four memory locations) containing the starting address of a section of code that is executed when the corresponding interrupt occurs. The section of code that is executed is called an Interrupt Service Routine (ISR).

Each interrupt vector consists of the low and high bytes of the ISR's segment address and low and high bytes of the ISR's address offset with the segment. These form the CS:IP values for the CPU to jump to when the corresponding interrupt occurs. Therefore, in 1 KB of memory, 256 different interrupt vectors may be stored. These are called interrupt types.

ISA DMA

ISA Direct Memory Access (DMA) cycles operate in single mode, since a DMA request initiates one DMA cycle in which one data transfer occurs. DMA allows the direct transfer of data from I/O devices to memory devices and vice versa (and from memory to memory) without involving the CPU. This makes it possible to transfer large amounts of data to and from memory in the background, at high speed.

The DMA system is based on two 8237-type DMA controllers. Controller 2 provides DMA channels 5, 6 and 7 as well as the cascade input for controller 1.

The 8237 device only supports 16-bit addresses (limiting access to 64 KB of memory). Each DMA channel has an associated page register on the main board to provide the additional addresses, so that up to 16 MB of memory may be accessed via DMA. This means that if more than 64 KB is to be transferred via DMA, the page register must be reprogrammed after each 64 KB block and a new block of DMA transfer started. This can lead to time gaps in the DMA transferred data if the data is arriving at high speed from a real-time data acquisition expansion board.

A technique called Dual Channel DMA can be used to overcome the problems with time gaps in the DMA transferred data. Two DMA channels are used in an alternating manner. Channel 1 is used first to transfer data into memory while Channel 2 is being programmed. When 64 KB of data has been transferred the second DMA channel is used and the first DMA channel is reprogrammed.

Notes

Chapter 2
Digital Signal Processing

Digital Signal Processing (DSP) is formally defined as a digital operation performed on an input sequence of numbers (including feedback from the result of the digital operation). The sequence of numbers can represent anything from digitised human speech to stock price data, processed to detect hidden periodicities or patterns.

Typical DSP operations include:

- Digital filtering (low-pass, bandpass, high-pass, bandstop and multiple-band filters).
- Discrete Fourier Transforms (especially the Fast Fourier Transforms) to analyze the periodic frequency content of a signal.
- Signal modulation (generation of sinusoidal waveforms).
- Autocorrelation (for analysis of periodic signals in a single-input signal).
- Cross-correlation (used to determine frequency and time relationships between two different but related signals).

Digital filtering and correllation techniques will be disussed in the following sections.

Digital Filtering

Digital filtering is a commonly used DSP procedure and is relatively easy to implement. A digital filter is a numerical procedure, or algorithm, that transforms a given sequence of numbers into a second sequence that has more desirable properties, such as less noise or distortion.

A digital filter consists of the interconnection of three simple elements: adders, multipliers and delays. The adder and multiplier are components that are readily implemented in the arithmetic logic unit of the computer. Delays are components that allow access to future and past values in the sequence.

When a filter produces a unit-sample response of infinite duration, it is called an Infinite Impulse Response (IIR) filter. As this requires a recursive structure (the output is a function of past outputs), the terms IIR and recursive are commonly accepted as interchangeable when applied to digital filters. An IIR filter can go to infinity if it enters an unstable state after a unit pulse at the input.

A filter with a finite unit-sample response is called a Finite Impulse Response (FIR) filter. The term is used interchangeably with non-recursive because the output is a function of inputs only. An exception is the frequency-sampling structure for FIR filters, which does require recursion for the required response. An FIR filter eventually settles back to zero after a unit pulse at the input.

Figure 2.1 illustrates the two types of filters. (Note that the z^{-1} is a shorthand method of indicating delays; it also has mathematical significance).

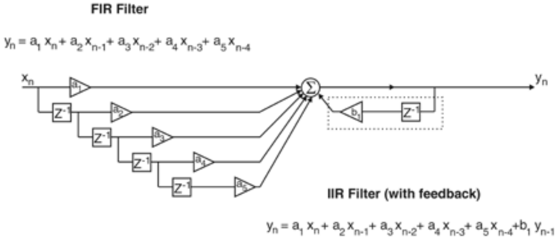


Figure 2.1
Representation of a digital filter

For example, if an analog voltage signate f(t) is sampled at discrete regular time intervals Δt as follows:

$$f(t),\ f(t+{}^{3}t),\ f(t+2{}^{3}t),\ldots\ldots f(t+k{}^{3}t)\ldots\ldots$$

and t=0 (to make it easier), the sequence of voltage samples becomes:

$$f(0),\ \ f(0+{}^{3}t),\ f(0+2{}^{3}t),\ldots\ldots f(0+k{}^{3}t)\ldots$$

This can be represented with the z transforms as:

$$f(0) + f(1)z^{-1} + f(2)z^{-2} + f(3)z^{-3} + \ldots\ldots\ldots\ f(k)z^{-k}$$

The variable z^{-k} can be interpreted as a type of operator that, upon multiplication, shifts signal samples to the right (delays) by k time units.

Figure 6.1 demonstrates how any discrete time (or digital) filter with input x(k) and output y(k) can be represented with the general difference equation:

$$b_0y(k) + b_1\ y(k-1) + \ldots + b_My(k-M) = a_0x(k) + a_1x(k-1) + \ldots + a_Nx(k-N)$$

Thus:

$$y_k = \sum_{i=o}^{N} a_i x_{k-i} - \sum_{i=1}^{M} b_i y_{k-i} \qquad 2.0$$

In combining these components, we get a filtered output y_n. The process of implementation of these equations, to a set of data, is therefore called digital filtering. The resultant equations are known as difference equations.

This means that input samples enter at the left end of the diagram and move to the right through each delay element as each new sample is ready. The newest input sample is x(k). The previous input sample delayed by one sample period is x(k-1). The sample before it is x(k-2) and so on. With each new sample, a sum of products cycle is performed in which current and past inputs are multiplied by their respective coefficients.

Taking the Z-transform of the above equation, this becomes:

$$Y(z)\,(1+\sum_{m=1}^{M} b_m z^{-m}) = X(z)\sum_{n=1}^{N} a_n z^{-n} \qquad 2.1$$

This means that X(z) and Y(z) are represented as:

$$X(z) = \sum_{k=0}^{\infty} x(k)\, z^{-k} \qquad 2.2$$

$$Y(z) = \sum_{k=0}^{\infty} y(k)\, z^{-k} \qquad 2.3$$

The discrete time (or digital) transfer function can thus be defined as:

$$H(z) = \frac{Y(z)}{X(z)} \qquad 2.4$$

$$H(z) = \frac{\sum_{n=0}^{N} a_n z^{-n}}{1 + \sum_{m=1}^{M} b_m z^{-m}} \qquad 2.5$$

This can also be written as:

$$Y(z) = H(z)X(z)$$

The output sequence is then obtained using the inverse z-transform.

A special case of this equation can be obtained for the unit pulse input sequence where:

$$x(k) = \begin{bmatrix} 1 & k = 0 \\ 0 & k \neq i \end{bmatrix} \qquad 2.6$$

which results in a Z-transform X(z)=1. The response to this input is therefore the inverse z-transform of H(z).

FIR filters have the advantage of being completely stable and possess linear phase shift. They use only past and current inputs and do not have any counterparts in the analog world. IIR filters produce better performance with fewer coefficients, but lack some of the advantages of the FIR filters. Because IIR filters use feedback of past outputs into the output, they can be unstable - although proper design overcomes the problem.

The coefficients, which dictate filter response, are usually based around the response of a filter to an impulse function (x_n=1 n=0, x_n=0<>0). By then working backwards from the impulse response, the coefficients (or transfer function) for the filter are deduced.

The non-recursive filter transfer function follows from Equation 6.7 for all bm$^{=0}$.

$$H(z) = \sum_{n=0}^{N} a_n z^{-n} \qquad 2.7$$

The corresponding difference equation is:

$$y(k) = \sum_{n=0}^{N} z_n x(k-n) \qquad 2.8$$

$$y_n = \sum_{i=0}^{N} a_i x(n-i) \qquad 2.9$$

With an impulse input:

$$x_n = \delta_n = \begin{bmatrix} 1 & n = 0 \\ 0 & n \neq 0 \end{bmatrix}$$

we get the output

$$y_n = h_n = \sum_{i=0}^{N} a_i \delta(n-i) \qquad 2.10$$

where

$$\delta(n-i) = \delta_{n-i} = \begin{bmatrix} 1 & n = i \\ 0 & n \neq i \end{bmatrix}$$

which gives

$$h_n = a_n$$

thus giving a more usable transfer function for a discrete system

$$H(z) = \sum_{i=0}^{N} h_i z^{-i} \qquad 2.11$$

where:

$$z = e^{jwT}$$

Knowing that the transfer function H(z) is a periodic function of frequency, and also knowing the frequency response that is required, the Fourier series can then be used to obtain the coefficient series hn.

$$c_n = \frac{1}{t} \int_{-t/2}^{+t/2} f(t) e^{-jn\omega_0 t} dt$$

2.12

$$f(t) = \sum_{n=-\infty}^{\infty} c_n e^{jnw_0 t}$$

2.13

where:

2š/w_0 is the period of f(t)

c_n is the frequency spectrum

Conversely, in reversing the time-frequency role, we get:

$$H(w) = \sum_n a_n e^{-jnwT}$$

2.14

$$a_n = \frac{1}{w_s} \int_{-\omega_s/2}^{+\omega_s/2} H(\omega) e^{jn\omega T} d\omega$$

2.15

where:

a_n is the time domain sequence of numbers for the impulse response

w_s is the sampling frequency

w_s equals 2š/T where T = sampling period

Using Nyquist's theorem, which states sampling frequency should be at least double the maximum frequency to be sampled, $\pm w_s /2$ is thus the maximum cutoff frequency, so:

$$h_n = \frac{1}{w_s} \int_{-w_c}^{w} H(w) e^{jnwT} dw \qquad 2.16$$

where:

w_c = cutoff frequency [RT1] $w_s/2$

But this is still an infinite series, as in Figure 2.2(a), since infinite coefficients will produce ideal filtering characteristics. A finite set of coefficients can be achieved by truncating the data with the introduction of a delay as in Figure 2.2(b) (delay of 5 increments), and then by setting to zero all coefficients that are less than zero or greater than N.

This delay will be carried to the output yn, with the relevant data only starting after N operations of the difference equation. Hence larger data sets are required, not only for resolution of the sampled signal, but for filters with a large number of coefficients there will be an equally long delay before the relevant output is achieved.

For example for an FIR filter with 100 coefficients and sampling rate of 1000 Hz for a signal of 100 Hz, this gives 10 points per one full waveform, thus requiring 100 samples to get the relevant filtering started and at least another 15 samples to get any useful filtering results at the output. Thus is the case, only 15 output points hold relevant data (one and a half periods properly filtered).

You can use the system from Figure 2.1 and Equation 2.16 to calculate a few coefficient values, assuming that:

- Sampling frequency f_s = 20 kHz and cutoff frequency f_c = 5 kHz (note that f_c $f_s/2$)
- $T = (1/20)*10^3 = 5*10^{-5}$ sec and w_c = 2š5000 rad/sec

Solving for h_n

$$h_n = \frac{1}{w_s} \int_{-w_c}^{w_c} H(w) e^{jnwT} = \frac{w_c T}{\pi} \frac{\sin n w_c T}{n w_c T} \qquad 2.17$$

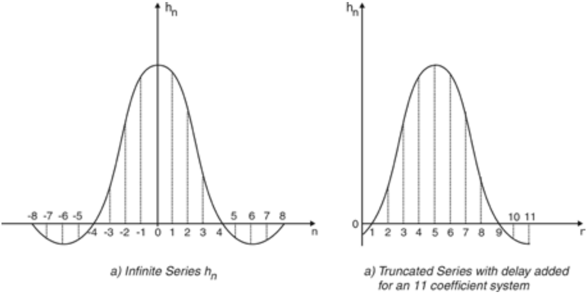


Figure 2.2
Infinite and truncated series

Entering the values of sampling period and cutoff frequency we get:

$$h_n = \frac{1}{2}\left(\frac{\sin n\frac{\pi}{2}}{n\frac{\pi}{2}}\right)$$

where $n = 1, \pm 1, \pm 2$

which gives $h_o = 0.5$

$h_1 = 0.318309 = h_{-1}$

$h_2 = 0 = h_{-2}$

Now inserting a delay of 2 and applying to a_1 - a_5:

$$h_2 = a_5 = a_1 = 0$$

$$h_1 = a_4 = a_2 = 0.318309$$

$$h_0 = a_3 = 0.5$$

Using a system with only five coefficients will give a poor filter response and (as mentioned earlier) the use of more coefficients will improve filter quality, though at the cost of more processing time. This type of filtering may be enhanced using suitable windowing functions (such as a Kaiser window or a Hamming window) which will modify the coefficients to give an improved filter performance.

The use of low-pass coefficients to find the coefficients for high-pass, bandpass and bandstop filters can be computed as follows:

Low-pass → high-pass

$$h_{n_{HP}}=(-1)^n h_{n_{LP}}$$

Low-pass → bandpass

$$h_{n_{BP}}=(2\cos\pi W_o T)h_{n_{LP}}$$

Bandpass → bandstop

$$h_{o_{BS}}=1-h_{o_{BP}} \text{also } -h_{n_{BS}}=-h_{n_{BP}} \; n=\pm 1,\pm 2,...$$

Correlation Techniques

Correlation is a process normally used for finding the presence of a periodic signal which is buried in noise. The main types of correlation are autocorrelation and cross-correlation.

Autocorrelation is the process of multiplying a frame of samples by the same frame which has been shifted.

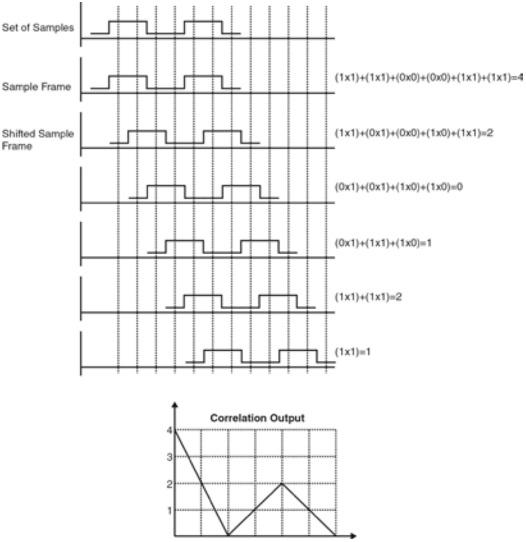


Figure 2.3
Graphical representation of auto correlation

As shown in Figure 2.3, the autocorrelated signal is made up from a sum of products of each shifted frame and the original frame, starting from zero shift until the full frame has been shifted.

An improvement in the Signal-to-Noise ratio (S/N) can be gained when this is applied to a more realistic signal, as shown in Figure 2.4.

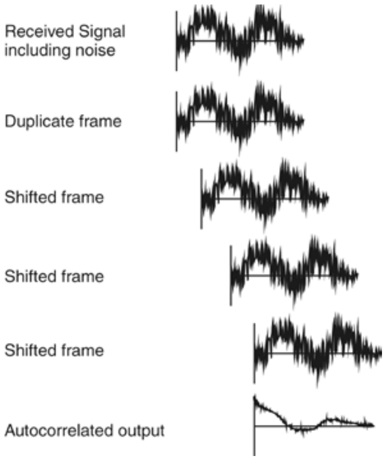


Figure 2.4
Graphical representation of autocorrelation with lower S/N

Cross-correlation is similar to autocorrelation, except that the sample frame is correlated with a known reference frame. This is used if the shape and frequency of the signal are known. Cross-correlation can be used to identify a known signal within a noisy sampled frame, as illustrated in Figure 2.5

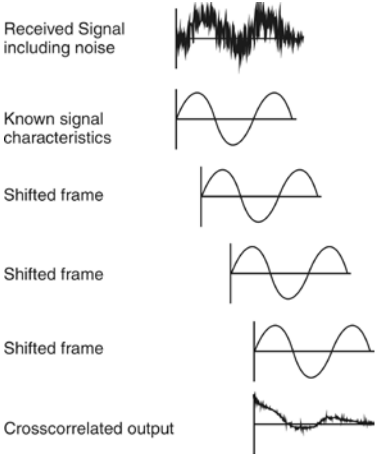


Figure 2.5
Graphical representation of cross-correlation

Notes

Chapter 3
Converting Analog to Digital Signals and Vice Versa

A Typical DSP System

Most of the signals encountered in engineering applications are analog. In order to process analog signals using digital techniques they must first be converted into digital signals.

Digital processing of analog signals proceeds in three stages:

- The analog signal is digitized.

  Digitization involves two processes: sampling (digitization in time) and quantization (digitization in amplitude). This whole process is called analog-to-digital (A/D) conversion.

- The digitized signal is processed.

  The digitized signal is processed by the appropriate DSP algorithms.

- The results or outputs of the processing

  The results or outputs of the processing are converted back into analog signals through interpolation. This process is called digital-to-analog (D/A) conversion.

Figure 3.1 illustrates these three stages in diagram form.

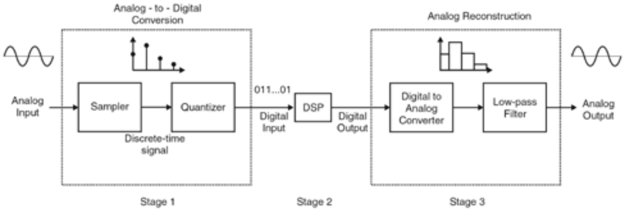


Figure 3.1
The Three Stages of Analog-Digital-Analog Conversions

Sampling

We shall first consider the sampling operation. It can be illustrated through the changing temperature through a single day. The continuous temperature variation is shown in Figure 3.2. However, the observatory may only be recording the temperature once every hour.

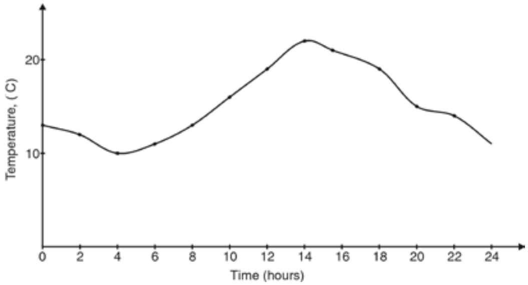


Figure 3.2
Temperature Variation Throughout a Day

The records are shown in Table 3.1. When we plot these values against time, we have a snapshot of the variation in temperature throughout the day. These snapshots are called samples of the signal (temperature). They are plotted as dots in Figure 3.2. In this case the sampling interval, the time between samples, is one hour.

Hour	***Temperature***
0	13
2	12
4	10
6	11
8	13
10	16
12	19
14	23
16	22
18	20
20	16
22	15
24	12

Table 3.1
Temperature Measured At Each Hour of A Day

Figure 3.3 shows the diagramatic representation of the sampling process.

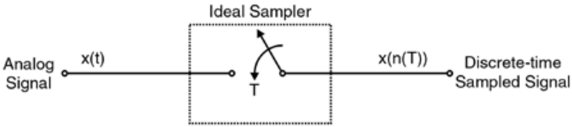


Figure 3.3
The Sampling Process

The analog signal is sampled once every T seconds, resulting in a sampled data sequence. The sampler is assumed to be ideal in that the value of the signal at an instant (an infinitely small time) is taken. A real sampler, of course, cannot achieve that and the "switch" in the sampler is actually closed for a finite, though very small, amount of time. This is analogous to a camera with a finite shutter speed. Even if a camera can be built with an infinitely fast shutter, the amount of light that can reach the film plane will be very small indeed. In general, we can consider the sampling process to be close enough to the ideal.

It should be pointed out that throughout our discussions we shall assume that the sampling interval is constant. In other words, the spacing between the samples is regular. This is called uniform sampling. Although irregularly sampled signals can, under suitable conditions, be converted to uniformly sampled ones, the concept and mathematics are beyond the scope of this introductory course.

The most important parameter in the sampling process is the sampling period T, or the sampling frequency or sampling rate fs which is defined as

$$f_s = \frac{1}{T}$$

Sampling frequency is given in units of "samples per second" or "Hertz". If the sampling is too frequent, then the DSP process will have to process a large amount of data in a much shorter time frame. If the sampling is too sparse, then important information might be missing in the sampled signal. The choice is governed by Sampling Theorem.

Sampling Theorem

The sampling theorem specifies the minimum sampling rate at which a continuous-time signal needs to be uniformly sampled so that the original signal can be completely recovered or reconstructed by these samples alone. This is usually referred to as Shannon's sampling theorem in the literature.

If a continuous time signal contains no frequency components higher than W Hz, then it can be completely determined by uniform samples taken at a rate f_s samples per second where

$$f_s \geq 2W$$

or, in terms of the sampling period

$$T \leq \frac{1}{2W}$$

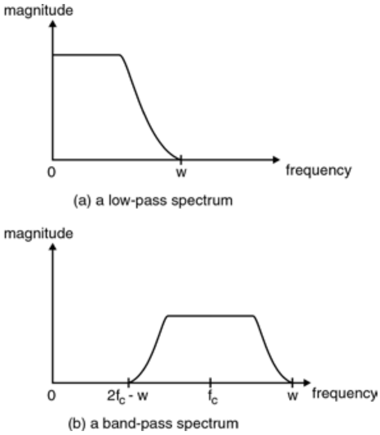


Figure 3.4
Two Bandlimited Spectra

A signal with no frequency component above a certain maximum frequency is known as a bandlimited signal. Figure 3.4 shows two typical bandlimited signal spectra: one low-pass and one band-pass.

The minimum sampling rate allowed by the sampling theorem ($f_s = 2W$) is called the Nyquist rate.

It is interesting to note that even though this theorem is usually called Shannon's sampling theorem, it was originated by both E.T. and J.M. Whittaker and Ferrar, all British mathematicians. In the Russian literature, this theorem was introduced to communications theory by Kotel'nikov and took its name from him. C.E. Shannon used it to study what is now known as Information Theory in the 1940's. Therefore in the mathematics and engineerng literature sometimes it is also called WKS sampling theorem after Whittaker, Kotel'nikov and Shannon.

Frequency Domain Interpretation

The sampling theorem can be proven and derived mathematically. However, a more intuitive understanding of it could be obtained by looking at the sampling process from the frequency domain perspective.

If we consider the sampled signal as an analog signal, it is obvious that the sampling process is equivalent to a very drastic chopping of the original signal. The sharp rise and fall of the signal amplitude just before and after the signal sample instants introduce a large amount of high frequency components into the signal spectrum.

It can be shown through the Fourier transform (which we will discuss in Chapter 4) that the high frequency components generated by sampling appear in a very regular fashion. In fact, every frequency component in the original signal spectrum is periodically replicated over the entire frequency axis. The period at which this replication occurs is determined by the sampling rate.

This replication can easily be justified for a simple sinusoidal signal. Consider a single sinusoid:

$$x(t) = \cos(2\pi f_c t)$$

Before sampling, the spectrum consists of a single spectral line at frequency fa. Sampling is performed at time instants

$$t=nT, \qquad n=0,1,2,K$$

where n is a positive integer. Therefore the sampled sinusoidal signal is given by

$$x(t)=x(nT)=\cos(2\pi f_a n T)$$

At a frequency

$$f = f_a + f_s$$

the sampled signal has value

$$x'(t) = \cos[2\pi (f_a + f_s)nT]$$
$$x'(t) = \cos[2\pi f_a nT + 2\pi f_s nT]$$
$$x'(t) = \cos[2\pi f_a nT + 2n\pi]$$
$$x'(t) = \cos[2\pi f_a nT]$$

which is the same as the original sampled signal. Hence we can say that the sampled signal has frequency components at

$$f = f_u + nf_s$$

This replication is illustrated in Figure 3.5.

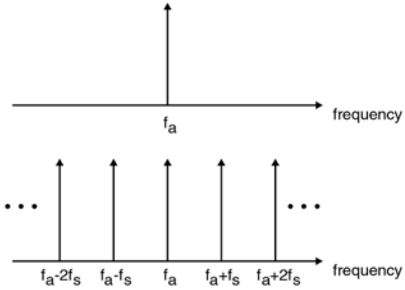


Figure 3.5
Replication of Spectrum through Sampling

Although it is only illustrated for a single sinusoid, the replication property holds for an arbitrary signal with an arbitrary spectrum. Replication of the signal spectrum for a low-pass bandlimited signal is shown in Figure 3.6.

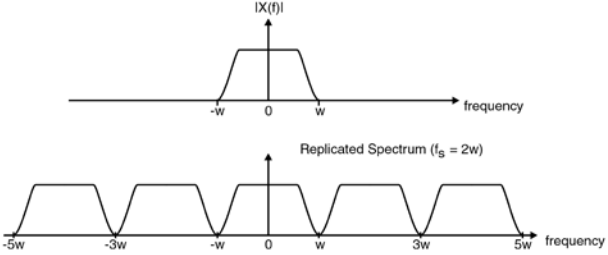


Figure 3.6
The Original Low-pass Spectrum and the Replicated Spectrum after Sampling

Consider the effect if the sampling frequency is less than twice the highest frequency component as required by the sampling theorem. As shown in Figure 3.7, the replicated spectra overlap each other, causing distortion to the original spectrum. Under this circumstance, the original spectrum can never be recovered faithfully. This effect is known as aliasing.

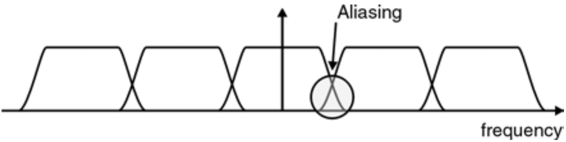


Figure 3.7
Aliasing

If the sampling frequency is at least twice the highest frequency of the spectrum, the replicated spectra do not overlap and no aliasing occurs. Thus the original spectrum can be faithfully recovered by suitable filtering.

Aliasing

The effect of aliasing on an input signal can be demonstrated by sampling a sine wave of frequency f_a using different sampling frequencies. Figure 3.8 shows such a sinusoidal function sampled at three different rates: $fs=4f_a$, $fs=2f_a$, and $fs=1.5f_a$.

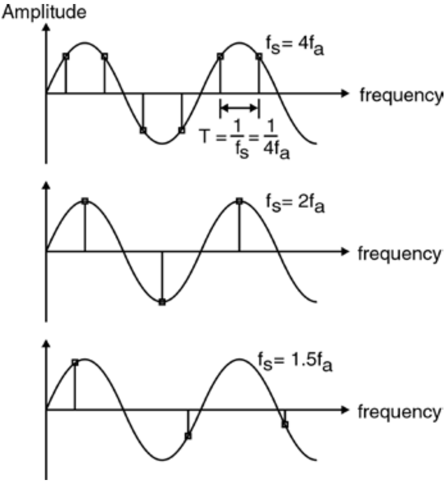


Figure 3.8
A Sinusoid Sampled at Three Different Rates

In the first two cases, if we join the sample points using straight lines, it is obvious that the basic "up-down" nature of the sinusoid is still preserved by the resulting triangular wave as shown in Figure 3.9.

If we pass this triangular wave through a low-pass filter, a smooth interpolated function will result. If the low-pass filter has the appropriate cut-off frequency, the original sine wave can be recovered.

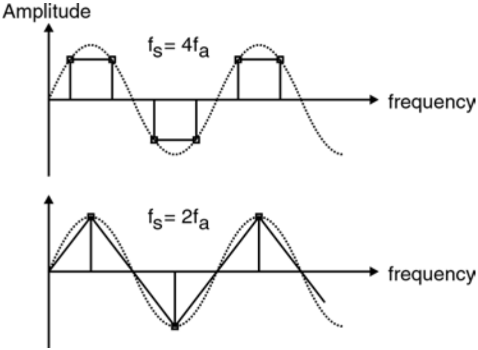


Figure 3.9
Interpolation of Sample Points with No Aliasing

For the last case in Figure 3.8, the sampling frequency is below the Nyquist rate. We would expect aliasing to occur. This is indeed the case. If we join the sampled points together, it can be observed that the rate at which the resulting function repeats itself differs from the frequency of the original signal. In fact, if we interpolate between the sample points, a smooth function with a lower frequency results, as shown in Figure 3.10.

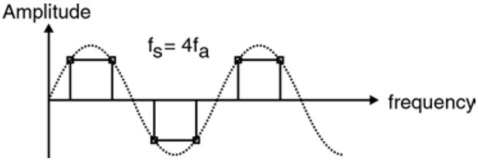


Figure 3.10
Effect of Aliasing

Therefore it is no longer possible to recover the original sine wave from these sampled points. We say that the higher frequency sine wave now has an "alias" in the lower frequency sine wave inferred from the samples. In other words, these samples are no longer representative of the input signal and therefore any subsequent processing will be invalid.

Notice that the Sampling Theorem assumes that the signal is strictly bandlimited. In the real world, typical signals have a wide spectrum and are not bandlimited in the strict sense. For instance, we may assume that 20kHz is the highest frequency the human ears can detect. Thus we want to sample at a frequency slightly above 40kHz (say, 44.1kHz as in compact discs) as dictated by the Sampling Theorem. However, the actual audio signals normally have a much wider bandwidth than 20kHz. We can ensure that the signal is bandlimited at 20kHz by low-pass filtering. This low-pass filter is usually called anti-alias filter.

Anti-aliasing Filters

Anti-aliasing filters are always analog filters as they process the signal before it is sampled. In most cases they are also low-pass filters unless bandpass sampling techniques are used. (Bandpass sampling will not be discussed here.)

The sampling process incorporating an ideal low-pass filter as the anti-alias filter is shown in Figure 3.11. The ideal filter has a flat passband and the cut-off is very sharp. Since the cut-off frequency of this filter is half of that of the sampling frequency, the resulting replicated spectrum of the sampled signal do not overlap each other. Thus no aliasing occurs.

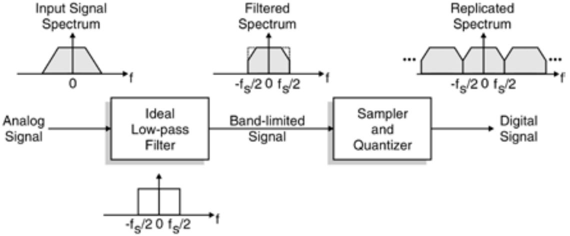


Figure 3.11
The Analog-to-Digital Conversion Process with Anti-alias Filtering

Practical low-pass filters cannot achieve the ideal characteristics. What are the implications? Firstly, this would mean that we have to sample the filtered signals at a rate that is higher than the Nyquist rate to compensate for the transition band of the filter. The bandwidth of a low-pass filter is usually defined as the 3-dB point (the frequency at which the magnitude response is 3dB below the peak level in the passband or at half the power). But signal levels below 3dB are still quite significant for most applications. For the audio signal application example in the previous section, it may be decided that signal levels below 40dB will cause insignificant aliasing. The anti-aliasing filter used may have a bandwidth of 20kHz but the response is 40dB down starting from 24kHz. This means that the minimum sampling frequency has to be increased to 48kHz instead of 40kHz for the ideal filter.

Alternatively, if we fix the sampling rate, then we need an anti-alias filter with a sharper cut-off. Using the same audio example, if we want to keep the sampling rate at 44.1kHz, the anti-aliasing filter will need to have an attenuation of 40dB at about 22kHz. With a bandwidth of 20kHz, the filter will need a transition from 3dB at down to 40dB within 2kHz. This typically means that a higher order filter will be required. A higher order filter also implies that more components are needed for its implementation.

Practical Limits on Sampling Rates

As discussed in previous sections, the practical choice of sampling rate is determined by two factors for a certain type of input signal. On one hand, the sampling theorem imposes a lower bound on the allowed values of the sampling frequency. On the other hand, the economics of the hardware imposes an upper bound. This economics includes the cost of the analog-to-digital converter (ADC) and the cost of implementing the analog anti-alias filter. A higher speed ADC will allow a higher sampling frequency but may cost substantially more. However, a lower sampling frequency will put a more stringent requirement on the cut-off of the anti-aliasing filter, necessitating a higher order filter and a more complex circuit which again may cost more.

In real-time applications, each sample is acquired (sampled), quantized and processed by a DSP. The output samples may need to be converted back to analog form. A higher sampling rate will means that there are more samples to be processed within a certain amount of time. If Tproc represents the total DSP chip

processing time, then the time interval between samples Ts will need to be greater than Tproc. Otherwise the processor will not be able to keep up. This means that if we increase the sampling rate we will need a higher speed DSP chip.

Mathematical Representation

A mathematical representation of the sampling process (and any other process involved in DSP for that matter) is needed so that we can describe precisely the process and to help us in the analysis of DSP.

The sampling process can be described as a multiplication of the analog signal with a periodic impulse function. This impulse function is also known as the Dirac delta function and is usually denoted by (t). It is shown in Figure 3.12.

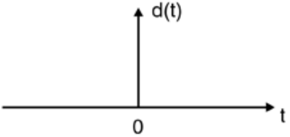


Figure 3.12
The Dirac Delta Function

It can be considered as a rectangular pulse with zero duration and infinite amplitude. It has the property that the energy, or the area under the pulse is equal to one. This is expressed as

$$\int_{-\infty}^{+\infty} \delta(t)dt = 1$$

Thus a weighted or scaled impulse function would be defined as one that satisfies

$$\int_{-\infty}^{+\infty} A\delta(t)dt = A$$

The weighted impulse function is drawn diagrammatically as an arrow with a height proportional to the scaling factor.

The periodic train of impulse functions is expressed as

$$s(t) = \ldots + \delta(t - 2T_s) + \delta(t - T_s) + \delta(t) + \delta(t + T_s) + \delta(t + 2T_s) + \ldots\ldots.$$

$$s(t) = \sum_{n=-\infty}^{n=+\infty} \delta(t - nT_s)$$

where T_s is the amount of time between two impulses. In terms of sampling, it is the sampling period.

If the input analog signal is denoted by f(t), then the sampled signal is given by

$$y(t) = f(t)s(t)$$

$$y(t) = \sum_{n=-\infty}^{n=+\infty} f(t).\delta(t - nT_s)$$

or the samples of the output of the sampling process are

$$y(nT_S) = f(nT_S) \bullet \delta(t\text{-}nT_S)$$

Sometimes the sampling period is understood and we just use y(n) to denote $y(nT_s)$.

This mathematical representation will be used again and again in later chapters of this course.

Quantization

Sample-and-Hold

The next step in the process of converting an analog signal into digital form is the discretization of the sampled signal amplitude or quantization. In practice, because the quantization process takes a finite amount of time, the sampled signal amplitude has to be held constant during this time. The sampling process is usually performed by a sample-and-hold circuit which can be logically represented as in Figure 3.13. The quantization process is performed by the analog-to-digital converter (hereinafter referred to as an ADC).

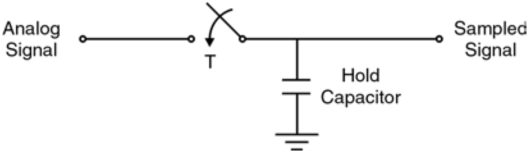


Figure 3.13
Sample and Hold Circuit

The hold capacitor holds the sampled measurement of the analog signal x(nT) for at most T seconds during which time a quantized value $x_Q(nT)$ is available at the output of the analog-to-digital converter, represented as a B-bit binary number. The sample-and-hold and the ADC may be separate modules or may be integrated on the same chip. Typically the very fast ADCs require an external sample-and-hold device.

Uniform Quantization

The ADC assumes that the input values cover a full-scale range, say R. Typical values of R are between 1 to 15 volts. Since the quantized sampled value $x_Q(nT)$ is represented by B-bits, it can take on only one of 2^B possible quantization levels. If the spacing between these levels is the same throughout the range R, then we have a uniform quantizer. The spacing between quantization levels is called the quantization width or the quantizer resolution.

For uniform quantization, the resolution is given by

$$Q = \frac{R}{2^B}$$

The number of bits required to achieve a required resolution of Q is therefore

$$B = \log_2 \frac{R}{Q}$$

Most ADCs can take bipolar inputs which means the sampled values lie within the symmetric range

$$-\frac{R}{2} \leq x(nT) < \frac{R}{2}$$

For unipolar inputs,

$$0 \leq x(nT) < R$$

In practice, the input signal x(t) must be preconditioned to lie within the full-scale range of the quantizer. Figure 3.14 shows the quantization levels of a 3-bit quantizer for bipolar inputs.

For a review of the possible binary representations for the quantized output value, see Appendix E.

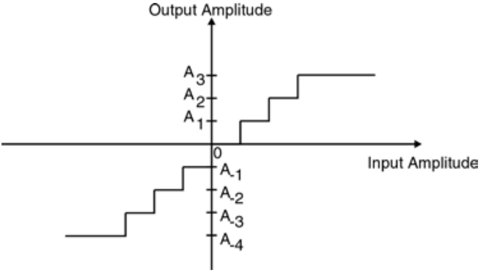


Figure 3.14
A Uniform 3-bit Quantizer Transfer Function

Quantization error is the difference between the actual sampled value and the quantized value. Mathematically, this is

$$e(nT) = x(nT) - x_Q(nT)$$

or equivalently,

$$e(n) = x(n) - x_Q(n)$$

If x(n) lies between two quantization levels, it will either be rounded up or truncated. Rounding replaces x(n) by the value of the nearest quantization level. Truncation replaces x(n) by the value of the level below it.

For rounding, the error is given by

$$-\frac{Q}{2} < e < \frac{Q}{2}$$

whereas for truncation, it is

$$0 \le e < Q$$

It is obvious that rounding produces a less biased representation of the analog values. The average error is given by

$$\bar{e} = \frac{1}{Q}\int_{-Q/2}^{Q/2} e\,de = 0$$

which means that on average half the values are rounded up and half down.

The mean-square value of the error gives us an idea of the average power of the error signal. It is given by

$$\overline{e^2} = \frac{1}{Q}\int_{-Q/2}^{Q/2} e^2\,de$$

The root-mean-square error is therefore

$$e_{rms} = \sqrt{\overline{e^2}}$$

$$= \frac{Q}{\sqrt{12}}$$

The signal-to-quantization-noise ratio is

$$SQNR = 20\log_{10}(\frac{R}{Q})$$

$$SQNR = 20\log\ 2^B$$

$$SQNR = 20B\log_{10} 2$$

$$SQNR = 6B\ \ dB$$

Thus if we increase the number of bits of the ADC by one, the signal to quantization noise ratio improves by 6 dB. The previous equation gives us the dynamic range of the quantizer.

Example:

The dynamic range of the human ear is about 100 dB. If a digital audio system is required to match this dynamic range, it will require

$$0100/6 = 16.67 \text{ bits}$$

A 16-bit quantizer will achieve a dynamic range of 96 dB.

If the highest frequency the human ear can hear is 20kHz, then a sampling rate of at least 40kHz is required. If the actual sampling rate is 44kHz, then the bit rate of this system will be

$$16.44 = 704 \text{ kbits/sec}$$

This is the typical bit rate of a compact disc player.

Since the quantization error is a random number within the range given, it is usually modelled as a random signal (or noise) with a uniform distribution as shown in Figure 3.15.

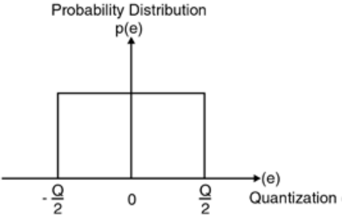


Figure 3.15
Uniform Distribution of Quantization Error

The quantized signal is then modelled as the analog sampled signal with additive quantization noise as in Figure 3.16. This quantization noise is generally assumed to be a zero-mean, uniformly distributed white noise that is uncorrelated with the input signal.

This assumption is generally true for signals that vary through the entire full-scale range and the quantizer has a large number of levels.

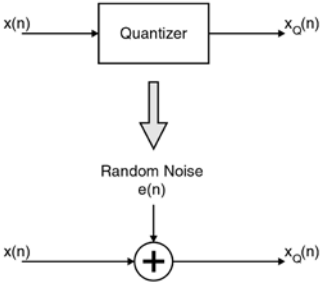


Figure 3.16
Mathematical Model of Quantization Noise

Non-uniform Quantization

One of the assumptions we have made in analysing the quantization error is that the sampled signal amplitude is uniformly distributed over the full-scale range. This assumption may not hold for certain applications. For instance, speech signals are known to have a wide dynamic range. Voiced speech (e.g. vowel sounds) may have amplitudes that span the whole full-scale range while softer unvoiced speech (e.g. consonants such as fricatives) usually have much smaller amplitudes. Also, an average person only speaks 60% of the time while she/he is talking. The remaining 40% is silence with a negligible signal amplitude.

If uniform quantization is used, the louder voiced sounds will be adequately represented. However, the softer sounds will probably occupy only a small number of quantization levels with similar binary values. This means that we would not be able to distinguish between the softer sounds. As a result, the reconstructed analog speech from these digital samples will not nearly be as intelligible as the original.

To get around this problem, non-uniform quantization can be used. More quantization levels are assigned to the lower amplitudes while the higher amplitudes will have less number of levels. This quantization scheme is shown in Figure 3.17.

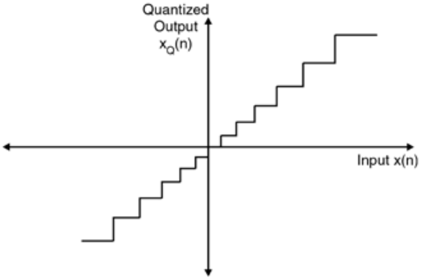


Figure 3.17
Non-uniform Quantization

Alternatively, a uniform quantizer can still be used, but the input signal is first compressed by a system with an input-output relationship (or transfer function) similar to that shown in Figure 3.18.

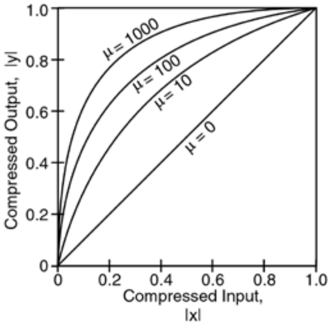


Figure 3.18
μ–*law Compression Characteristics*

The higher amplitudes of the input signal are compressed, effectively reducing the number of levels assigned to it. The lower amplitude signals are expanded (or non-uniformly amplified), effectively making it occupy a large number of quantization levels. After processing, an inverse operation is applied to the output signal (expanding it). The system that expands the signal has an input-output relationship that is the inverse of the compressor. The expander expands the high amplitudes and compresses the low amplitudes. The whole process is called companding (COMpressing and exPANDING).

Companding is widely used in public telephone systems. There are two distinct companding schemes. In Europe, A-law companding is used and in the United States, μ - law companding is used.

$$y = y_{\max} \frac{\ln(1+\mu(\frac{|x|}{x_{\max}}))}{\ln(1+\mu)} \operatorname{sgn}(x)$$

where

$$\operatorname{sgn}(x) = \begin{cases} +1, & x \geq 0 \\ -1, & x < 0 \end{cases}$$

Here, x and y represent the input and output values, and x_{max} and y_{max} are the maximum positive excursions of the input and output, respectively. μ is a positive constant. The North American standard specifies μ to be 255. Notice that μ = 0 corresponds to a linear input-output relationship (i.e. uniform quantization). The compression characteristic is shown in Figure 3.18.

The A-law compression characteristic is given by

$$y = \left[y_{\max} \frac{A(\frac{[x]}{x_{\max}})}{1+\ln A} \operatorname{sgn}(x), 0 < \frac{[x]}{x_{\max}} \leq \frac{1}{A} \right]$$

$$y = \left[y_{\max} \frac{1+\ln[A(\frac{[x]}{x_{\max}})]}{1+\ln A} \operatorname{sgn}(x), \frac{1}{A} < \frac{[x]}{x_{\max}} \leq 1 \right]$$

Here, A is a postive constant. The European standard specifies A to be 87.6. Figure 3.19 shows the characteristic graphically.

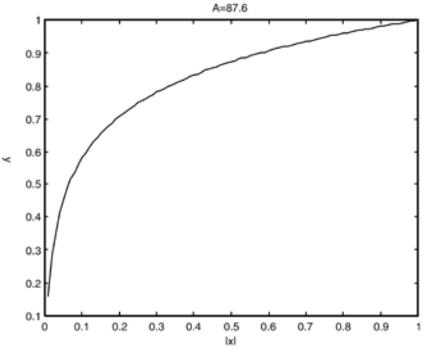


Figure 3.19
The A-law Compression Characteristics

Dithering

Another assumption we have made in analysing quantization noise is that it is assumed to be uniformly distributed over the quantization width. If the noise is not uniformly distributed, quantization distortion results.

We shall illustrate quantization distortion through an example. A low amplitude sinusoid is being sampled and quantized. The samples of the sinusoid are given by

$$x(n) = A\cos(2\pi\ f_0 n)$$

where A is less than the quantization resolution. Let

f_s = 40 samples per cycle

and

A = 0.75Q

So for a 1 kHz sinusoid, the actual sampling rate is 40 kHz. Figure 3.20(a) shows the original and the quantized signals.

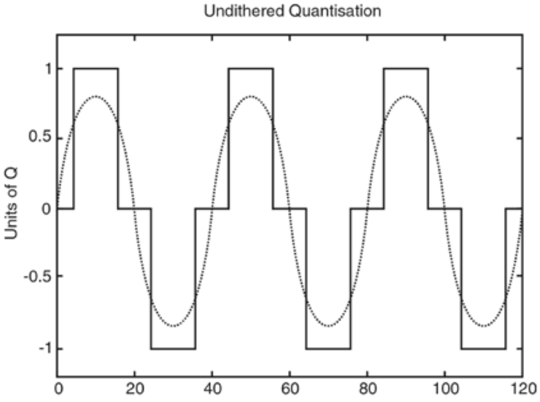


Figure 3.20 (a)
The Original and Quantized Signal

Note that the quantized signal only occupies three of the available quantization levels. The frequency spectrum of this quantized signal is shown in Figure 3.20(b).

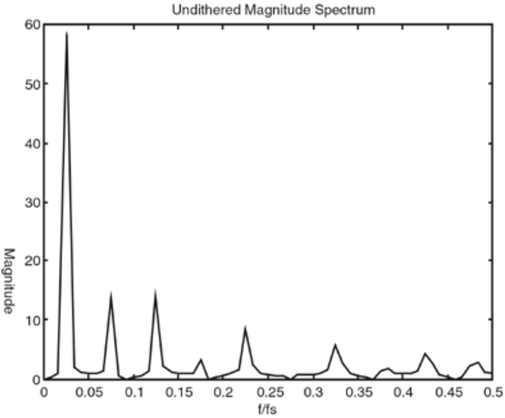


Figure 3.20 (b)
The Quantized Signal Spectrum

It has peaks at f0, and the odd harmonic frequencies 3f0, 5f0, etc. Clearly the odd harmonics are artefacts of the quantization process and can be considered as the spectrum of the quantization noise signal which, in this case, is not white.

This problem can be overcome by adding a dither v(n) to the original sampled signal so that

$$y(n) = x(n) + v(n)$$

Various types of dither can be added. Two of them which are of practical interest are rectangular and triangular dither. They are so called because the distribution of the random signal samples are rectangular and triangular in shape respectively. The distributions are shown in Figure 3.21.

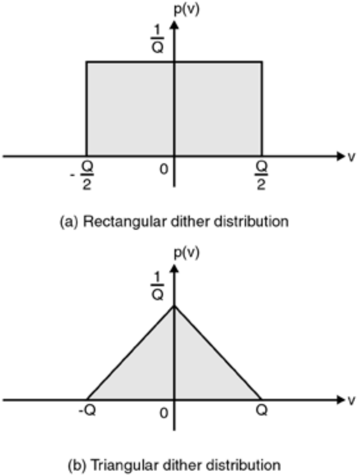


Figure 3.21
Amplitude Distributions of Rectangular and Triangular Dither

The addition of dither to the original signal will increase its average quantization noise power. Recall that the average noise power for uniform quantization is $Q^2/12$. The addition of rectangular dither will double this average noise power and the addition of triangular dither will triple it. However, if we look at the frequency spectrum of the dithered and quantized signal of the example we have been considering (Figure 3.22), we will notice that the noise spectrum now appears to be white and the odd harmonic artefacts are not there any more.

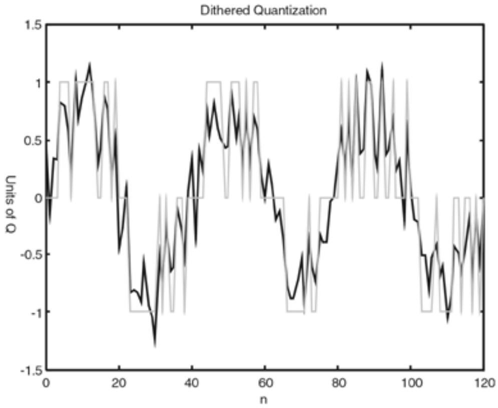


Figure 3.22(a)
The Dithered Signal and Its Quantized Version

It must be emphasized that in general, the sampling process will cause all the odd harmonics that lie outside of the Nyquist interval (out-of-band harmonics) to be aliased back into the interval (in-band non-harmonic frequencies). So the overall spectrum will contain peaks at frequencies other than the odd harmonics.

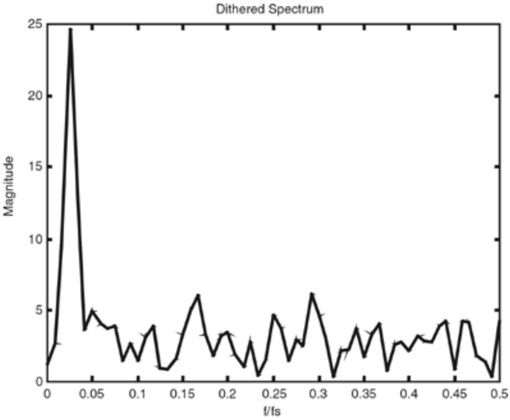


Figure 3.22(b)
Quantization Noise Spectrum with Dithering

Analog-to-Digital Converters

We have covered the fundamental process of converting analog signals to digital format so that they can be digitally processed. The analog signal is first low-pass filtered to half the sampling frequency to prevent aliasing. It then goes through a sample-and-hold device and the sampled amplitudes are quantized and converted to binary values. This binary number is represented by n bits where n is typically 8, 10, 12 and 16. Appendix E reviews the three main types of binary representation.

Now we shall take a brief look at some commercially available analog-to-digital converters (ADCs). There are many varieties of ADCs available on the market. Most of them contain the sample-and-hold circuitry. They cover a wide range of conversion speeds, resolution (number of bits representing the output), and input voltage range. Some are general purpose and others are for specific applications such as video signals. Different methods of quantization are used. Four most common methods are discussed here.

Successive Approximation

The successive approximation ADC is built from three main blocks: a analog-to-digital converter (DAC), a successive approximation register (SAR) and a comparator. Figure 3.23 shows how these three blocks are connected.

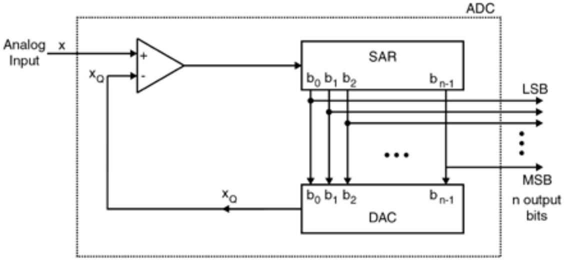


Figure 3.23
Successive Approximation Converter

The conversion process is as follows. Initially all n bits are reset to zero in the SAR. Starting with the most significant bit (MSB) bn-1, each bit is set to 1 in sequence. The DAC converts the newly formed binary number into a corresponding voltage which is compared with the input voltage. If the input voltage exceeds the DAC output, then that bit will be left on. Otherwise it will be reset to zero (off). After n cycles, the SAR will hold the correct bit pattern which is then latched on to the output lines. This technique thus basically keeps splitting the voltage range in half to determine where the input voltage lies. Alternatively, we can say that the successive approximation algorithm performs a binary search through the quantization levels.

Example:

Convert an analog values x=0.2 and x=-0.7 volts to their offset binary representations using successive approximation. Assume a 3-bit quantizer with a range R=2V.

For 3-bit quantization the conversion will be done in 3 cycles. The bit that is tested, the corresponding quantized value of the intermediate bit pattern and the test results are tabulated below for x=0.2V.

Cycle	***Test bit***	***b2b1b0***	x_Q	***Test result***
1	b2	100	0.00	1
2	b1	110	0.50	0
3	b0	101	0.25	0
		100	0.00	

For the test result column, a "1" indicates the input is larger than or equal to the DAC output and a "0" otherwise. In cycle 2, the test result is a "0", thus the SAR will reset b1 back to zero. Similarly in cycle 3, b0 is reset to zero, resulting in the output of "100" representing the quantized voltage of 0.00.

The following table reflects the conversion process for x=-0.7V.

Cycle	***Test bit***	***b2b1b0***	x_Q	***Test result***
1	b2	100	0.00	0
2	b1	010	-0.50	0
3	b0	011	-0.75	1

The resulting quantized value is -0.75V and is encoded as "011".

Notice that in the example, both values are truncated down to the lower level. If rounding to the nearest level is desired, then the input value x must be shifted by half the spacing (resolution) between levels. That is, obtain the shifted value y by

$$y = x + Q/2$$

and quantize y by successive approximation.

Many ADCs also give a two's complement output. If this is the output format required, the successive approximation algorithm has to be slightly modified. This is because the MSB (i.e. the sign bit) must be treated separately from the other bits. If the input value is greater than zero, the MSB must be set to "0"; otherwise, it is a "1". Note that this is the opposite to the offset binary case. The remaining bits are tested in the usual manner.

Example:

Perform the quantization as in the previous example but use two's complement representation.

For x=0.2, the process is illustrated in the following table:

Cycle	Test bit	b2b1b0	xQ	Test result
1	b2	000	0.00	1
2	b1	010	0.50	0
3	b0	001	0.25	0
		000	0.00	

The resulting binary value is "000".

The following table illustrates the quantization of x= -0.7 to two's complement:

Cycle	Test bit	b2b1b0	xQ	Test result
1	b2	000	0.00	0
2	b1	110	-0.50	0
3	b0	101	-0.75	1
		101	-0.75	

The two's complement representation is "101".

Notice that complementing the MSB (sign bit) will give us the offset binary representation.

A large number of ADCs that operates at sampling frequencies of 1 MHz or less make use of successive approximation.

Dual Slope ADC

If a higher resolution (than for successive approximation, for example) is desired, then the dual slope conversion technique can be employed. A key element of the dual slope ADC is a capacitor. At the start of the conversion cycle, the capacitor is totally discharged (i.e. the capacitor voltage is zero). It is then charged for a certain set time by the input voltage. After this set time the capacitor is switched to a known negative reference voltage and is slowly discharged until the capacitor voltage reaches zero volt. The time taken for the discharge process is recorded

using a digital counter. With the counter initially set to zero, the final counter value is proportional to the input voltage. The binary counter value is the converted binary output.

High resolution conversion can be achieved by simply using a more accurate counter which is relatively easy to implement. Another advantage of this process is that component value variations will have no effect on the accuracy. For instance, the capacitance may change due to temperature variation. But since the charging and discharging processes are done through the same capacitor, the net effect of this capacitance variation is negligible.

The major disadvantage is that the charging and discharging of capacitors takes a relatively long time. So this process is normally reserved for high resolution, low sampling frequency ADCs.

Flash ADC

For n-bit quantization, the successive approximation technique requires n cycles. If fast conversion time is required, the comparisons will have to be performed in parallel and at the same time. In flash ADCs, the input voltage is compared with a set of reference voltages at the same time. These reference voltages are set by a ladder of resistors with equal resistances.

For an n-bit converter, we need 2^n resistors. The voltages tapped from the terminals of these resistors are then compared with the input voltage and the digital output encoded. Figure 3-24 shows a 2-bit flash ADC.

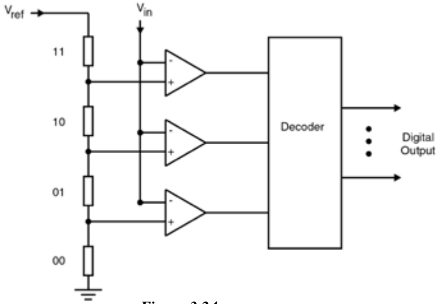


Figure 3.24
A 2-Bit Flash ADC

In practice, each resistor in the ladder must be matched and laser trimmed to the same value for accuracy. This is a very costly process. Thus flash ADCs are usually expensive and are available only up to 8 bits (with 256 resistors).

Sigma-Delta ADC

The concept of Sigma-Delta converters is significantly different to the above three techniques. A Sigma-Delta ADC features a very low resolution quantizer (typically 1-bit quantization) but operates with a sampling rate much, much higher than the Nyquist rate (oversampling). Recall that if the sampling frequency is increased, then the requirements on the anti-aliasing filter is relaxed.

Another advantage of oversampling is that the quantization noise power is now spread over a much larger frequency range. More precisely, if fs is the sampling frequency, noise power is spread from -fs/2 to fs/2. Since the input signal occupies a frequency band much narrower than this range, the noise power affecting the input signal is lower.

One-bit quantization is used in a modulation technique in communication systems called Delta modulation. It basically quantizes the difference between successive samples of the signal rather than the absolute value of each sample.

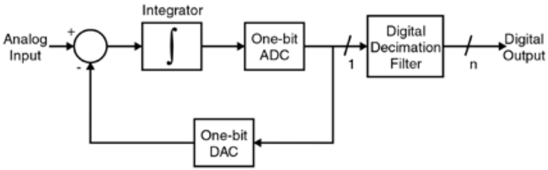


Figure 3.25
A Sigma-Delta ADC

A block diagram of a sigma-delta converter is shown in Figure 3-25. The term "Sigma-Delta" comes from the fact that there is a summation point (sigma) and a delta modulator (integrator and 1-bit quantizer). Analysis of this system can be quite involved. The noise performance is frequency dependent. The loop acts as a low-pass filter for the input signal and a high-pass filter for the quantization noise. This noise-shaping property is especially suitable for digital audio applications.

The 1-bit output of the quantizer is decimated which is a reduction in sampling rate. This rate reduction is performed by averaging a block of n-bits to produce a one-bit output. This averaging process is illustrated in Figure 3-26. This rate reduction is equivalent to filtering in the frequency domain and is discussed at a later chapter.

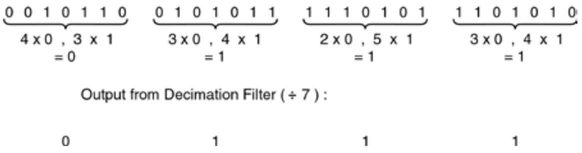


Figure 3.26
Averaging a Block of 7 Bits to Produce 1 Bit

As we have seen, the majority of the processes involved in sigma-delta conversion are digital processes. This means that the chip contains mostly of digital circuitry as opposed to the other three techniques which have a significant portion of analog circuitry. Thus sigma-delta ADCs are generally more reliable and stable. It is also possible for this type of ADC to be integrated with the DSP core, reducing the chip count, enhancing system reliability and reducing overall cost.

Analog Reconstruction

There are applications where the information that we are looking for can be extracted from the digitally processed signal. In this case, there is no need to produce an output that is analog. So stage 3 in Figure 2-1 does not exist. An example is a receiver for digitally modulated signals. The aim of the receiver is the detection of digital symbols being transmitted. The input to the receiver is the carrier modulated signal and the output is the sequence of detected symbols.

However, there are many applications that require the construction of analog waveforms or signals from the digital signal in the form of a sequence of numbers. Intuitively what we want is to "fill in the gaps" or to interpolate between the sampled values so that a continuous-time signal results.

This is performed by an analog reconstructor as shown in Figure 3-27.

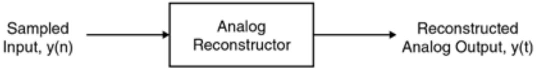


Figure 3.27
Analog Signal Reconstruction

Generally speaking, any form of interpolation will do the job. But there are some interpolation methods that are easiler to implement and are, in some ways, more desirable than others.

We shall discuss two kinds of reconstructors. The first one is ideal. As the name suggests, this kind of reconstructors is not practical and in fact is not physically implementable. But it reflects the ideal situation and will help us to understand the process better. The second type is called a staircase reconstructor. They are simple to implement and are in fact most commonly used in practical analog-to-digital converters.

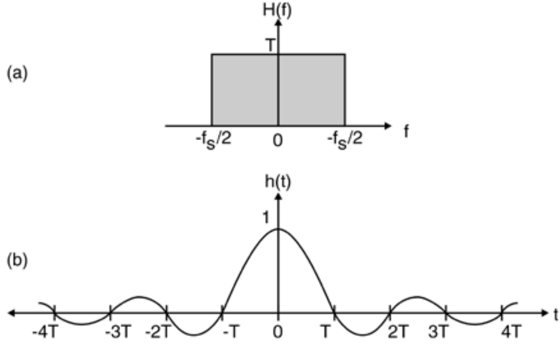
Ideal Reconstructor

Let us consider an analog signal x(t) with a frequency spectrum X(f) that has been sampled at the rate of 1/T samples per second. The sampled signal x(n) will have a spectrum that consists of replica of X(f) shifted by integer multiples of fs. Assume that the spectrum X(f) is bandlimited and the sampling rate is sufficiently high so that its replica do not overlap. Then X(f) can be recovered by a low-pass filter with a cutoff frequency of fs/2.

Ideally, this low-pass filter will have frequency characteristics

$$H(f) = \begin{bmatrix} T, & for \quad |f| \leq f_s/2 \\ 0, & otherwise \end{bmatrix}$$

so that there is no distortion to the spectrum in the Nyquist interval and no frequency component outside this interval is included. H(f) is shown graphically in Figure 3-28(a).



Figures 3.28(a) and 3.28(b)
An Ideal Low-pass Filter and Its Impulse Response

The time-domain characteristic corresponding to H(f) is given by

$$h(t) = \frac{\sin(\pi\ t / T)}{\pi\ t / T}$$

$$h(t) = \sin c(\pi\ t / T)$$

$$h(t) = \sin c(\pi\ f_s t)$$

which is known as the sinc function. It is shown in Figure 3-28(b).

Notice that h(t) is not physically realizable. This is because it is non-causal. A causal system is one that if excited at t=0 will produce a response starting from t=0. Since h(t) is non-zero in the negative frequency axis, it is non-causal. It means that if this low-pass filter is excited by a single impulse at t=0, the response will have started even before the excitation arrives at the input. Clearly this is not possible for a real system. So we cannot implement an ideal reconstructor.

Staircase Reconstructor

The reconstructor that is often used in practice is the staircase reconstructor or zero-order hold (ZOH). This reconstructor simply holds the value of the most recent sample until the next sample arrives. So each sample value is held for T seconds. This is illustrated in Figure 3-29(a).

The ZOH can be characterized by the impulse response

$$h_{ZOH}(t) = 1, \quad for\ 0 \le t \le T$$
$$\qquad\qquad 0, \quad otherwise$$

This means that if the reconstructor is excited by an impulse at t=0, the output of the reconstructor will be a rectangular waveform with an amplitude equal to that of the impulse with a duration of T seconds.

It is obvious that the resulting staircase output will contain some high frequency components because of the abrupt change in signal levels. In fact, the spectrum of hZOH(t) is a sinc function that is decaying exponentially in amplitude.

$$H_{ZOH}(f) = T\frac{\sin(\pi f T)}{\pi f T}e^{-j\pi f T}$$

It is shown in Figure 3-29(b) in comparison to the spectrum of the ideal reconstructor. It is obvious that parts of the replicas of the baseband spectrum are included in the output of the ZOH. Figure 3-30 shows the spectra at the input and output of the ZOH.

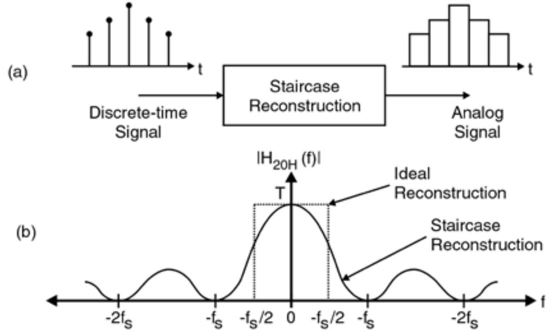


Figure 3.29(a) and 3.29(b)
Analog Reconstruction Using Zero Order Hold

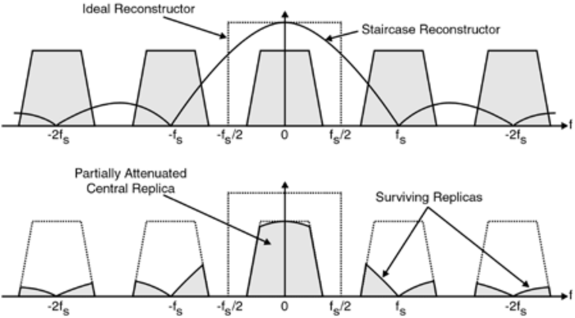


Figure 3.30
Spectra at the Input and Output of the Zero Order Hold

Image-Rejection Postfilters

The inclusion of some of the replicas of the baseband spectrum will lead to distortion. It is therefore desirable that they be removed. Since the sampling rate is sufficiently high, the baseband spectrum can be isolated by low-pass filtering.

A low-pass filter that removes the remaining replicated spectra is also known as an image-rejection filter. The cutoff frequency of this filter should clearly be fs/2. It is very similar to the anti-aliasing filter in characteristics.

Even though the replicated spectra are completely removed (rejected), the baseband spectrum is still slightly distorted by both the ZOH and the image-rejection filter. At the frequency fs/2, the ZOH introduces an attenuation of about 4dB and the image-rejection filter another 3dB. While this may be acceptable for some applications, it is highly undesirable for other applications such as high quality digital audio.

This problem can be overcome by equalization. The equalizer has a frequency characteristic HEQ(f) so that the combined frequency response of the equalizer, staircase reconstructor, and the image-rejection filter will be the ideal response H(f). That is,

$$H_{EQ}(f)H_{ZOH}(f)H_{post}(f) = H(f)$$

where $H_{post}(f)$ is the frequency characteristics of the image-rejection filter.

The advantage of using DSP is that the equalizer can actually be implemented digitally. In other words, the original digital signal samples are first digitally pre-compensated before being converted to analog signal.

Digital-to-Analog Converters

Digital-to-analog converters (DACs) are the implementations of the reconstructors. Since DACs are much simpler than ADCs, they are correspondingly cheaper. A digital binary code is converted to an analog output which may be a current or voltage. Figure 3-31 shows the schematic of an n-bit DAC.

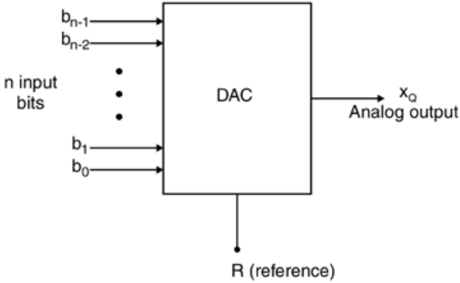


Figure 3.31
An n-Bit DAC

An important parameter for ADC is the conversion time - the time it takes for the device to obtain a stable quantized value from the time the conversion starts. For a DAC, the corresponding parameter is the settling time - the delay between the binary data appearing at the input and a stable voltage being obtained at the output.

Multiplying DAC

The most common DACs are multiplying DACs. The name arises because the output is the sum of the products of the binary code and current sources. Each bit of the binary code turns on or off a corresponding current source. The sum of all the currents available can be converted to a voltage for output or remain as is. Figure 3-32 shows such a current source multiplying DAC. The current sources are normally on and are grounded when not in use.

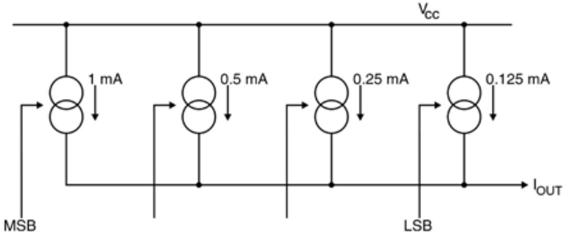


Figure 3.32
A Current Source Multiplying DAC

A voltage source can be used instead of current sources. The voltage source is applied to a series of scaled resistors. The voltages at one end of the resistors are either switched "on" or "off" as shown in Figure 3-33. The "on" voltages are summed. The output is proportional to the weighted sum of the input voltages. Some devices have a built-in reference voltage source. Other ones allow the user to provide an external reference voltage, thereby setting the accuracy of the output.

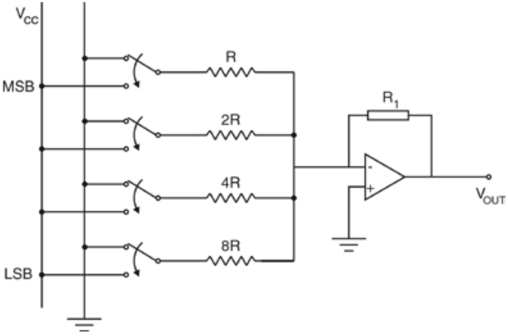


Figure 3.33
A Voltage Source Multiplying DAC

Nearly all commonly used DACs are ZOH devices and therefore image-rejection filters are needed. The settling time of multiplying DACs are short because the conversion is done in parallel.

Bit Stream DAC

A disadvantage of a multiplying DAC is that the most significant bit (MSB) must be very accurate. This accuracy will be required for the whole range of temperatures specified for the device. Furthermore, it has to be consistent over time.

For an 8-bit DAC, the MSB must be accurate to one part in 2^8=256. The MSB of a 16-bit DAC will need to be accurate to one part in 2^{16}=65536. Otherwise, some of the least significant bits will be rendered useless and the true resolution of the DAC will diminish. Maintaining voltage and current sources to this level of accuracy is not easy.

One way of overcoming this problem is to use bit stream conversion techniques. The concept is similar to sigma-delta ADCs. In bit stream DACs, a substantially higher sampling frequency is used in exchange for a smaller number of quantization levels.

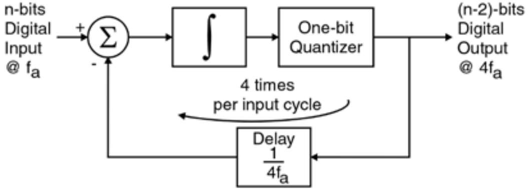


Figure 3.34
The Oversampling Stage of a Bit Stream DAC

Figure 3-34 shows the input oversampling stage of a particular bit-stream DAC. The input to this stage is an n-bit digital input sampled at a frequency fa and the output is an (n-2)-bit data sequence sampled at 4fa. The difference between the current digital input and the digital output is computed. The integrator is digital and simply adds the previous value to the present one. The output of the integrator is quantized into (n-2) bits by truncating the two least significant bits. This loss of

resolution is compensated for by the feedback of the output to the input and also the fact that this operation is performed four times for each digital input sample.

In general, for an n-bit input and a q-bit quantizer, the oversampling frequency will need to be 2^{n-q} times the original sampling rate. For some practical DACs, the output of this oversampling stage is a 1-bit representation of the input signal. This bit stream, if plotted against time and with sample points joined togther, is equivalent to a pulse density modulated (PDM) waveform as shown in Figure 3-35. This bit stream is converted to an analog signal by a 1-bit DAC and subsequently low-pass filtered.

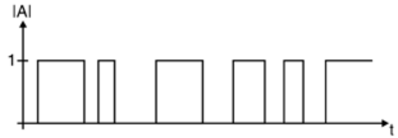


Figure 3.35
A Pulse Density Modulated Waveform

Owing to the fact that the original digital signal is being requantized into a small number of levels, the output can sometimes be "stuck" at an incorrect value. This happens most often when there is a long sequence of the same input value. This "hang-up" will persist until the next change in input value. The result of this "hang-up" is that the output will have a substantially different DC (or average) value to that of the input signal.

To overcome this problem, a dithering signal can be added. The effect of dithering has been discussed in Section 2.3.4. In this case, dithering lowers the probability of long sequences of any one value.

A further problem with bit stream techniques is the high oversampling frequency. For instance, if we want to resample a CD quality audio to one bit, then we need a frequency of $2^{16} \times 44.1 \times 10^3$ (approximately 3 GHz). This is a very high sampling frequency and is very difficult to implement using present silicon technology. In these cases, 1-bit DAC is not practical. Eventually, the design is a compromise between sampling rate and the number of bits required for the DAC.

To Probe Further

Sampling and data conversion is an extensive topic. We can only cover the basics here. There are some very good books describing the analog-to-digital and digital-to-analog conversion techniques in detail. Two of them are listed below:

D.H. Sheingold (ed.). *Analog-Digital Conversion Handbook, 3rd edition.* Prentice-Hall, 1986.

G.B. Clayton. *Data Converters*. Wiley, 1982.

We have discussed the sampling of a low-pass signal. The minimum sampling frequency is twice that of the bandwidth of the signal. If the signal to be sampled is a bandpass signal, we do not normally want to sample at twice the frequency of the highest frequency component of this signal since much of the lower frequency components are useless. This lead to the topic of bandpass sampling. Bandpass sampling is of particular interest to applications in carrier modulated communication systems. A good survey of results can be found in the following paper:

R.G. Vaughan and N.L. Scott, "*The Theory of Bandpass Sampling*", IEEE Transactions on Signal Processing, Vol.39, no.9, September 1991, pp.1973-1983.

For those who want to understand dithering further, the following two papers are suggested:

L. Schuchman, "*Dither Signals and Their Effect on Quantization Noise*", IEEE Transactions on Communications, Vol.COM-12, pp.162.165, 1964.

S.P. Lipshitz, R.A. Wannamaker and J. Vanderkooy, "*Quantization and Dither: A Theoretical Survey*", Journal of the Audio Engineering Society, Vol.40, 1992.

Many semiconductor manufacturers produce ADCs and DACs. They come in a variety of configurations. Product information can be obtained from the relevant databooks and the manufacturer's Web sites. Some of them provide customers with product information on CDs. They can usually be obtained from the locate distributors.

Contact the Manufacturers

Below is an incomplete list of manufacturers and their Web sites:

1. Analog Devices, Inc.	http://www.analog.com
2. Motorola, Inc.	http://www.motorola.com
3. National Semiconductors, Inc.	http://www.natsemi.com
4. Texas Instruments, Inc.	http://www.ti.com

Appendix A
Glossary of Terms

10BASE2	IEEE802.3 (or Ethernet) implementation on thin coaxial cable (RG58/AU).
10BASE5	IEEE802.3 (or Ethernet) implementation on thick coaxial cable.
10BASET	IEEE802.3 (or Ethernet) implementation on unshielded 22 AWG twisted pair cable.
A/D Conversion Time	This is the length of time a board requires to convert an analog signal into a digital value. The theoretical maximum speed (conversions/second) is the inverse of this value. See Speed/Typical Throughput.
A/D	Analog to Digital conversion.
Absolute Addressing	A mode of addressing containing both the instruction and location (address) of data.
Accuracy	Closeness of indicated or displayed value to the ideal measured value.
ACK	Acknowledge (ASCII - control F).
Acknowledge	A handshake line or protocol code which is used by the receiving device to indicate that it has read the transmitted data.
Active Device	Device capable of supplying current for a loop.
Active Filter	A combination of active circuit devices (usually amplifiers), with passive circuit elements (resistors and capacitors), which have characteristics that more closely match ideal filters than do passive filters.
Actuator	Control element or device used to modulate (or vary) a process parameter.
Address	A normally unique designator for location of data or the identity of a peripheral device which allows each device on a single communications line to respond to its own message.
Address Register	A register that holds the address of a location containing a data item called for by an instruction.
AFC	Automatic Frequency Control. The circuit in a radio receiver that automatically keeps the carrier frequency centred in the passband of the filters and demodulators.
AGC	Automatic Gain Control. The circuit in a radio that automatically keeps the carrier gain at the proper level.

Algorithm	Can be used as a basis for writing a computer program. This is a set of rules with a finite number of steps for solving a problem.
Alias Frequency	A false lower frequency component that appears in data reconstructed from original data acquired at an insufficient sampling rate (less than two times the maximum frequency of the original data).
ALU	see Arithmetic Logic Unit.
Amplitude Modulation	A modulation technique (also referred to as AM or ASK) used to allow data to be transmitted across an analog network, such as a switched telephone network. The amplitude of a single (carrier) frequency is varied or modulated between two levels; one for binary 0 and one for binary 1.
Analog	A continuous real-time phenomenon in which the information values are represented in a variable and continuous waveform.
Analog Input Board	Printed Circuit Board which converts incoming analog signals to digital values.
ANSI	American National Standards Institute. The principle standards development body in the USA.
Apogee	The point in an elliptical orbit that is furtherest from earth.
Appletalk	A proprietary computer networking standard initiated by Apple Computer for use in connecting the Macintosh range of computers and peripherals (including Laser Writer printers).
	This standard operates at 230 kilobits/second.
Application Program	A sequence of instructions written to solve a specific problem facing organisational management.
	These programs are normally written in a high-level language and draw on resources of the operating system and the computer hardware in executing its tasks.
Application Layer	The highest layer of the seven layer ISO/OSI Reference Model structure, which contains all user or application programs.
Arithmetic Logic Unit	The element(s) in a processing system that perform(s) the mathematical functions such as addition, subtraction, multiplication, division, inversion, AND, OR, NAND and NOR.
ARP	Address Resolution Protocol. A Transmission Control Protocol/ Internet Protocol (TCP/IP) process that maps an IP address to Ethernet address, required by TCP/IP for use with Ethernet.
ARQ	Automatic Request for Transmission. A request by the receiver for the transmitter to retransmit a block or a frame because of errors detected in the originally received message.
AS	Australian Standard.

ASCII	American Standard Code for Information Interchange. A universal standard for encoding alphanumeric characters into 7 or 8 binary bits. Drawn up by ANSI to ensure compatibility between different computer systems.
ASIC	Application Specific Integrated Circuit.
ASK	Amplitude Shift Keying. See Amplitude Modulation.
ASN.1	Abstract Syntax Notation One. An abstract syntax used to define the structure of the protocol data units associated with a particular protocol entity.
Asynchronous	Communications in which characters can be transmitted at an arbitrary, unsynchronised time, and where the time intervals between transmitted characters may be of varying lengths. Communication is controlled by start and stop bits at the beginning and end of each character.
Attenuation	The decrease in signal magnitude or strength between two points.
Attenuator	A passive network that decreases the amplitude of a signal (without introducing any undesirable characteristics to the signals such as distortion).
AUI CABLE	Attachment Unit Interface Cable. Sometimes called the drop cable to attach terminals to the transceiver unit.
Auto Tracking Antenna	A receiving antenna that moves in synchronism with the transmitting device which is moving (such as a vehicle being telemetered).
Autoranging	An autoranging board can be set to monitor the incoming signal and automatically select an appropriate gain level based on the previous incoming signals.
AWG	American Wire Gauge.
Background Program	An application program that can be executed whenever the facilities of the system are not needed by a higher priority program.
Backplane	A panel containing sockets into which circuit boards (such as I/O cards, memory boards and power supplies) can be plugged.
Balanced Circuit	A circuit so arranged that the impressed voltages on each conductor of the pair are equal in magnitude but opposite in polarity with respect to a defined reference.
Band Pass Filter	A filter that allows only a fixed range of frequencies to pass through. All other frequencies outside this range (or band) are sharply reduced in magnitude.
Band Reject	A circuit that rejects a defined frequency band of signals while passing all signals outside this frequency range (both lower than and higher than).

Bandwidth	The range of frequencies available, expressed as the difference between the highest and lowest frequencies, in hertz (cycles per second, abbreviated Hz).
Bar Code Symbol	An array of rectangular parallel bars and spaces of various widths designed for the labelling of objects with unique identifications. A bar code symbol contains a leading quiet zone, a start character, one or more data characters including, in some cases, a check character, a stop character, and a trailing quiet zone.
Base Address	A memory address that serves as the reference point. All other points are located by offsetting in relation to the base address.
Base Band	Base Band operation is the direct transmission of data over a transmission medium without the prior modulation on a high frequency carrier band.
Base Loading	An inductance situated near the bottom end of a vertical antenna to modify the electrical length. This aids in impedance matching.
Baud	Unit of signalling speed derived from the number of events per second (normally bits per second). However, if each event has more than one bit associated with it, the baud rate and bits per second are not equal.
Baudot	Data transmission code in which five bits represent one character. Sixty-four alphanumeric characters can be represented.
BCC	Block Check Character. Error checking scheme with one check character; a good example being Block Sum Check.
BCD	Binary Coded Decimal. A code used for representing decimal digits in a binary code.
BEL	Bell (ASCII for control-G).
BERT/BLERT	Bit Error Rate/Block Error Rate Testing. An error checking technique that compares a received data pattern with a known transmitted data pattern to determine transmission line quality.
Bifilar	Two conducting elements used in parallel (such as two parallel wires wound on a coil form).
Binary Coded Decimal	(BCD) A code used for representing decimal digits in a binary code.
BIOS	The basic input/output system for the computer, usually firmware-based. This program handles the interface with the PC hardware and isolates the Operating Software (OS) from the low-level activities of the hardware. As a result, application software becomes more independent of the particular specifications of the hardware on which it runs, and hence more portable.

Bipolar Range / Inputs	A signal range that includes both positive and negative values. Bipolar inputs are designed to accept both positive and negative voltages. (Example: ±5 V).
Bisynchronous Transmission	See BSC.
Bit Stuffing with Zero Bit Insertion	A technique used to allow pure binary data to be transmitted on a synchronous transmission line. Each message block (frame) is encapsulated between two flags which are special bit sequences. Then if the message data contains a possibly similar sequence, an additional (zero) bit is inserted into the data stream by the sender, and is subsequently removed by the receiving device. The transmission method is then said to be data transparent.
BIT (Binary Digit)	Derived from "BInary DigiT", a one or zero condition in the binary system.
Bits & Bytes	One bit is one binary digit, either a binary 0 or 1. One byte is the amount of memory needed to store each character of information (text or numbers). There are eight bits to one byte (or character), and there are 1024 bytes to one kilobyte (KB). There are 1024 kilobytes to one megabyte (MB).
Block	In block-structured programming languages, a section of programming languages or a section of program coding treated as a unit.
Block Sum Check	This is used for the detection of errors when data is being transmitted. It comprises a set of binary digits (bits) which are the modulo 2 sum of the individual characters or octets in a frame (block) or message.
BNC	Bayonet type coaxial cable connector.
bps	Bits per second. Unit of data transmission rate.
Bridge	A device to connect similar sub-networks without its own network address. Used mostly to reduce the network load.
Broad Band	A communications channel that has greater bandwidth than a voice grade line and is potentially capable of greater transmission rates.
Broadcast	A message on a bus intended for all devices which requires no reply.
BS	Backspace (ASCII Control-H).
BS	British Standard.
BSC	Bisynchronous Transmission. A byte or character oriented communication protocol that has become the industry standard (created by IBM). It uses a defined set of control characters for synchronised transmission of binary coded data between stations in a data communications system.

Bubble Memory	Describes a method of storing data in memory where data is represented as magnetized spots called magnetic domains that rest on a thin film of semiconductor material. Normally used in high-vibration, high-temperature or otherwise harsh industrial environments.
Buffer	An intermediate temporary storage device used to compensate for a difference in data rate and data flow between two device (also called a spooler for interfacing a computer and a printer).
Burst Mode	A high speed data transfer in which the address of the data is sent followed by back to back data words while a physical signal is asserted.
Bus	A data path shared by many devices, with one or more conductors for transmitting signals, data or power.
Byte	A term referring to eight associated bits of information; sometimes called a "character".
Cache Memory	A fast buffer memory that fits between the CPU and the slower main memory to speed up CPU requests for data.
Capacitance (mutual)	The capacitance between two conductors with all other conductors, including shield, short circuited to the ground.
Capacitance	Storage of electrically separated charges between two plates having different potentials. The value is proportional to the surface area of the plates and inversely proportional to the distance between them.
Cascade	Two or more electrical circuits in which the output of one is fed into the input of the next one.
Cassegrain Antenna	Parabolic antenna that has a hyperbolic passive reflector situated at the focus of the parabola.
CCD	Charge-Coupled Device (camera).
CCIR	Comité Consultatif Internationale des Radiocommunications.
CCITT	Consultative Committee International Telegraph and Telephone. An international association that sets worldwide standards (e.g. V.21, V.22, V.22bis).
Cellular Polyethylene	Expanded or "foam" polyethylene consisting of individual closed cells suspended in a polyethylene medium.
CGA	Color Graphics Adapter. A computer standard utilising digital signals offering a resolution of 320 by 200 pixels and a palette of 16 colors.
Channel Selector	In an FM discriminator the plug-in module which causes the device to select one of the channels and demodulate the subcarrier to recover data.
Character	Letter, numeral, punctuation, control figure or any other symbol contained in a message..

Characteristic Impedance	The impedance that, when connected to the output terminals of a transmission line of any length, makes the line appear infinitely long. The ratio of voltage to current at every point along a transmission line on which there are no standing waves.
Clock	The source of timing signals for sequencing electronic events such as synchronous data transfer or CPU operation in a PC.
Clock Pulse	A rising edge, then a falling edge (in that order) such as applied to the clock input of an 8254 timer/counter.
Clock	The source(s) of timing signals for sequencing electronic events eg synchronous data transfer.
Closed Loop	A signal path that has a forward route for the signal, a feedback network for the signal and a summing point.
CMRR	Common Mode Rejection Ratio - A data acquisition's board's ability to measure only the voltage difference between the leads of a transducer, rejectingwhat the leads have in common. The higher the CMRR, the better the accuracy.
CMV	Common Mode Voltage.
CNR	Carrier to Noise Ratio. An indication of the quality of the modulated signal.
Cold-junction Compensation	Thermocouple measurements can easily be affected by the interface the thermocouples are connected to. Cold-junction compensation circuitry compensates for inaccuracies introduced in the conversion process.
Collector	The voltage source in a transistor with the base as the control source and the emitter as the controlled output.
Collision	The situation when two or more LAN nodes attempt to transmit at the same time.
Common Carrier	A private data communications utility company that furnishes communications services to the general public.
Common Mode Signal	The common voltage to the two parts of a differential signal applied to a balanced circuit.
Commutator	A device used to effect time-division multiplexing by repetitive sequential switching.
Compiler	A program to convert high-level source code (such as BASIC) to machine code-executable form, suitable for the CPU.
Composite Link	The line or circuit connecting a pair of multiplexers or concentrators; the circuit carrying multiplexed data.
Composite	A video signal that contains all the intensity, color and timing information necessary for a video product.

Conical Scan Antenna	An automatic tracking antenna system in which the beam is steered in a circular path so that it forms a cone.
Contention	The facility provided by the dial network or a data PABX which allows multiple terminals to compete on a first come, first served basis for a smaller number of computer ports.
Control System	A system in which a series of measured values are used to make a decision on manipulating various parameters in the system to achieve a desired value of the original measured values.
Convolution	An image enhancement technique in which each pixel is subjected to a mathematical operation that groups it with its nearest neighbours and calculates its value accordingly.
Correlator	A device which compares two signals and indicates the similarity between the two signals.
Counter/ Timer Trigger	On-board counter/timer circuitry can be set to trigger data acquisition at a user-selectable rate and for a particular length of time.
Counter Data Register	The 8-bit register of an (8254 chip) timer/counter that corresponds to one of the two bytes in the counter's output latch for read operations and count register for write operations.
CPU	Central Processing Unit.
CR	Carriage Return (ASCII control-M).
CRC	Cyclic Redundancy Check. An error-checking mechanism using a polynomial algorithm based on the content of a message frame at the transmitter and included in a field appended to the frame. At the receiver, it is then compared with the result of the calculation that is performed by the receiver. Also referred to as CRC-16.
Cross Talk	A situation where a signal from a communications channel interferes with an associated channel's signals.
Crossed Pinning	Wiring configuration that allows two DTE or DCE devices to communicate. Essentially it involves connecting pin 2 to pin 3 of the two devices.
Crossover	In communications, a conductor which runs through the cable and connects to a different pin number at each end.
Crosstalk	A situation where a signal from a communications channel interferes with an associated channel's signals.
CSMA/CD	Carrier Sense Multiple Access/Collision Detection. When two devices transmit at the same time on a local area network,they both cease transmission and signal that a collision has occurred. Each then tries again after waiting for a random time period.

Current Sink	This is the amount of current the board can supply for digital output signals. With 10-12 mA or more of current sink capability, a board can turn relays on and off. Digital I/O boards with less than 10-12 mA of sink capability are designed for data transfer only, not for hardware power relay switching.
Current Loop	A communication method that allows data to be transmitted over a longer distance with a higher noise immunity level than with the standard RS-232C voltage method. A mark (a binary 1) is represented by current; and a space (or binary 0) is represented by the absence of current.
Current Inputs	A board rated for current inputs can accept and convert analog current levels directly, without conversion to voltage.
D/A	Digital to Analog.
DAS	Data Acquisition System.
Data Integrity	A performance measure based on the rate of undetected errors.
Data Reduction	The process of analysing a large quantity of data in order to extract some statistical summary of the underlying parameters.
Data Link Layer	This corresponds to layer 2 of the ISO Reference Model for open systems interconnection. It is concerned with the reliable transfer of data (no residual transmission errors) across the data link being used.
Data Integrity	A performance measure based on the rate of undetected errors.
Datagram	A type of service offered on a packet-switched data network. A datagram is a self contained packet of information that is sent through the network with minimum protocol overheads.
dBi	A unit that is used to represent the gain of an antenna compared to the gain of an isotropic radiator.
dBm	A signal level that is compared to a 1-mW reference.
dBmV	A signal amplitude that is compared to a 1-mV reference.
dBW	A signal amplitude that is compared to a 1-Watt reference.
DCE	Data Communications Equipment. Devices that provide the functions required to establish, maintain and terminate a data transmission connection. Normally it refers to a modem.
Decibel	A logarithmic measure of the ratio of two signal levels where $dB = 20\log_{10} V_1/V_2$. Being a ratio, it has no units of measure.
Decibel (dB)	A logarithmic measure of the ratio of two signal levels where $dB = 20\log_{10} V_1/V_2$ or where $dB = 10\log_{10} P_1/P_2$ and where V refers to Voltage or P refers to Power. Note that it has no unit of measure.

Decoder	A device that converts a combination of signals into a single signal representing that combination.
Decommutator	Equipment for the demultiplexing of commutated signals.
Default	A value or setup condition assigned automatically unless another is specified.
Delay Distortion	Distortion of a signal caused by the frequency components making up the signal having different propagation velocities across a transmission medium.
DES	Data Encryption Standard.
Deviation	A movement away from a required value.
DFB	Display Frame Buffer.
Diagnostic Program	A utility program used to identify hardware and firmware defects related to the PC.
Dielectric Constant (E)	The ratio of the capacitance using the material in question as the dielectric, to the capacitance resulting when the material is replaced by air.
Differential	See Number of channels.
Digital	A signal which has definite states (normally two).
Digitize	The transformation of an analog signal to a digital signal.
DIN	Deutsches Institut Fur Normierung.
DIP	Acronym for dual in line package referring to integrated circuits and switches.
Diplexing	A device used to allow simultaneous reception or transmission of two signals on a common antenna.
Direct Memory Access	A technique of transferring data between the computer memory and a device on the computer bus without the intervention of the microprocessor. Also abbreviated to DMA.
Discriminator	Hardware device to demodulate a frequency modulated carrier or subcarrier to produce analog data.
Dish Antenna	An antenna in which a parabolic dish acts a reflector to increase the gain of the antenna.
Dish	Concave antenna reflector for use at VHF or higher frequencies.
Diversity Reception	Two or more radio receivers connected to different antennas to improve signal quality by using two different radio signals to transfer the information.
DLE	Data Link Escape (ASCII character).
DMA	Direct Memory Access.

DNA	Distributed Network Architecture.
Doppler	The change in observed frequency of a signal caused by the emitting device moving with respect to the observing device.
Downlink	The path from a satellite to an earth station.
DPI	Dots per Inch.
DPLL	Digital Phase Locked Loop.
DR	Dynamic Range. The ratio of the full scale range (FSR) of a data converter to the smallest difference it can resolve. DR = 2^n where n is the resolution in bits.
DRAM	Dynamic Random Access Memory. See RAM.
Drift	A gradual movement away from the defined input/output condition over a period of time.
Driver Software	A program that acts as the interface between a higher level coding structure and the lower level hardware/firmware component of a computer.
DSP	Digital Signal Processing.
DSR	Data Set Ready. An RS-232 modem interface control signal which indicates that the terminal is ready for transmission.
DTE	Data Terminal Equipment. Devices acting as data source, data sink, or both.
Dual-ported RAM	Allows acquired data to be transferred from on-board memory to the computer's memory while data acquisition is occurring.
Duplex	The ability to send and receive data over the same communications line.
Dynamic Range	The difference in decibels between the overload or maximum and minimum discernible signal level in a system.
EBCDIC	Extended Binary Coded Decimal Interchange Code. An 8-bit character code used primarily in IBM equipment. The code allows for 256 different bit patterns.
EEPROM	Electrically Erasable Programmable Read Only Memory. This memory unit can be erased by applying an electrical signal to the EEPROM and then reprogrammed.
EGA	Enhanced Graphics Adapter. A computer display standard that provides a resolution of 640 by 350 pixels, a palette of 64 colors, and the ability to display as many as 16 colors at one time.
EIA	Electronic Industries Association. An organisation in the USA specialising in the electrical and functional characteristics of interface equipment.

EIA-232-C	Interface between DTE and DCE, employing serial binary data exchange. Typical maximum specifications are 15m at 19200 Baud.
EIA-423	Interface between DTE and DCE, employing the electrical characteristics of unbalanced voltage digital interface circuits.
EIA-449	General purpose 37 pin and 9 pin interface for DCE and DTE employing serial binary interchange.
EIA-485	The recommended standard of the EIA that specifies the electrical characteristics of drivers and receivers for use in balanced digital multipoint systems.
EIRP	Effective Isotropic Radiated Power. The effective power radiated from a transmitting antenna when an isotropic radiator is used to determine the gain of the antenna.
EISA	Enhanced Industry Standard Architecture.
EMI/RFI	Electro-Magnetic Interference or Radio Frequency Interference. Background 'noise' capable of modifying or destroying data transmission.
EMS	Expanded Memory Specification.
Emulation	The imitation of a computer system performed by a combination of hardware and software that allows programs to run between incompatible systems.
Enabling	The activation of a function of a device by a defined signal.
Encoder	A circuit which changes a given signal into a coded combination for purposes of optimum transmission of the signal.
ENQ	Enquiry (ASCII Control-E).
EOT	End of Transmission (ASCII Control-D).
EPROM	Erasable Programmable Read Only Memory. Non-volatile semiconductor memory that is erasable in a ultra violet light and reprogrammable.
Equalizer	The device which compensates for the unequal gain characteristic of the signal received.
Error Rate	The ratio of the average number of bits that will be corrupted to the total number of bits that are transmitted for a data link or system.
Error	The difference between the setpoint and the measured value.
ESC	Escape (ASCII character).
ESD	Electrostatic Discharge.
Ethernet	Name of a widely used Local Area Network (LAN), based on the CSMA/CD bus access method (IEEE 802.3).
ETX	End of Text (ASCII control-C).

Even Parity	A data verification method normally implemented in hardware in which each character (and the parity bit) must have an even number of ON bits.
External Pulse Trigger	Many of the A/D boards allow sampling to be triggered by a voltage pulse from an external source.
Fan In	The load placed on a signal line by a logic circuit input.
Fan Out	The measure of drive capability of a logic circuit output.
Farad	Unit of capacitance whereby a charge of one coulomb produces a one volt potential difference.
FCC	Federal Communications Commission (USA).
FCS	Frame Check Sequence. A general term given to the additional bits appended to a transmitted frame or message by the source to enable the receiver to detect possible transmission errors.
FDM	Frequency Division Multiplexer. A device that divides the available transmission frequency range in narrower bands, each of which is used for a separate channel.
Feedback	A part of the output signal being fed back to the input of the amplifier circuit.
Field	One half of a video image (frame) consisting of 312.5 lines (for PAL). There are two fields in a frame. Each is shown alternately every 1/25 of a second (for PAL).
FIFO	First in, First Out.
Filled Cable	A telephone cable construction in which the cable core is filled with a material that will prevent moisture from entering or passing along the cable.
FIP	Factory Instrumentation Protocol.
Firmware	A computer program or software stored permanently in PROM or ROM or semi-permanently in EPROM.
Flame Retardancy	The ability of a material not to propagate flame once the flame source is removed.
Floating	An electrical circuit that is above the earth potential.
Flow Control	The procedure for regulating the flow of data between two devices preventing the loss of data once a device's buffer has reached its capacity.
Frame	A full video image comprising two fields. A PAL frame has a total of 625 lines (an NTSC frame has 525 lines).
Frame	The unit of information transferred across a data link. Typically, there are control frames for link management and information frames for the transfer of message data.

Frame Grabber	An image processing peripheral that samples, digitizes and stores a camera frame in computer memory.
Frequency Modulation	A modulation technique (abbreviated to FM) used to allow data to be transmitted across an analog network where the frequency is varied between two levels - one for binary '0' and one for binary '1'. Also known as Frequency Shift Keying (or FSK).
Frequency	Refers to the number of cycles per second.
Frequency Domain	The displaying of electrical quantities versus frequency.
Fringing	The unwanted bordering of an object or character with weak colors when there should be a clearly delineated edge.
Full Duplex	Simultaneous two way independent transmission in both directions (4 wire). See Duplex.
G	Giga (metric system prefix - 10^9).
Gain of Antenna	The difference in signal strengths between a given antenna and a reference isotropic antenna.
Gain	Amplification; applied to an incoming signal, gain acts as a multiplication factor on the signal, enabling a board to use signals that would otherwise be too weak. For example, when set to a gain of 10, a board with a range of +5 V can use raw input signals as low as +0.5 V (+500 mV); with a gain of 20, the range extends down to +250 mV.
Gateway	A device to connect two different networks which translates the different protocols.
Genlock	This is the process of synchronising one video signal to a master reference, ensuring that all signals will be compatible or related to one another.
Geostationary	A special earth orbit that allows a satellite to remain in a fixed position above the equator.
Geosynchronous	Any earth orbit in which the time required for one revolution of a satellite is an integral portion of a sidereal day.
GPIB	General Purpose Interface Bus. An interface standard used for parallel data communication, usually used for controlling electronic instruments from a computer. Also designated IEEE-488 standard.
Graphics Mode	In graphics mode each pixel on a display screen is addressable, and each pixel has a horizontal (or X) and a vertical (or Y) co-ordinate.
Grey Scale	In image processing, the range of available grey levels. In an 8-bit system, the grey scale contains values from 0 to 255.

Ground	An electrically neutral circuit having the same potential as the earth. A reference point for an electrical system also intended for safety purposes.
Half Duplex	Transmissions in either direction, but not simultaneously.
Half Power Point	The point in a Power versus frequency curve which is half the power level of the peak power (also called the 3dB point).
Hamming Distance	A measure of the effectiveness of error checking. The higher the Hamming Distance (HD) index, the safer is the data transmission.
Handshake Lines	Dedicated signals which allow two different devices to exchange data under asynchronous hardware control.
Handshaking	Exchange of predetermined signals between two devices establishing a connection.
Harmonic	An oscillation of a periodic quantity whose frequency is an integral multiple of the fundamental frequency. The fundamental frequency and the harmonics together form a Fourier series of the original wave form.
Harmonic Distortion	Distortion caused by the presence of harmonics in the desired signal.
HDLC	High Level Data Link Control. The international standard communication protocol defined by ISO to control the exchange of data across either a point-to-point data link or a multidrop data link.
Hertz (Hz)	A term replacing cycles per second as a unit of frequency.
Hex	Hexadecimal.
Hexadecimal Number	A base 16 number system commonly used with microprocessor systems.
HF	High Frequency.
High Pass	Generally referring to filters which allow signals above a specified frequency to pass but attenuate signals below this specified frequency.
High-Pass Filter	See HPF.
Histogram	A graphic representation of a distribution function, such as frequency, by means of rectangles whose widths represent the intervals into which the range of observed values is divided and whose heights represent the number of observations occurring in each interval.
Horn	A moderate-gain wide-beamwidth antenna.
Host	This is normally a computer belonging to a user that contains (hosts) the communication hardware and software necessary to connect the computer to a data communications network.
HPF	High-Pass Filter. A filter processing one transmission band that extends from a cutoff frequency (other than zero) to infinity.

HPIB	Hewlett-Packard Interface Bus; trade name used by Hewlett-Packard for its implementation of the IEEE-488 standard.
I/O Address	A method that allows the CPU to distinguish between different boards in a system. All boards must have different addresses.
IEC	International Electrotechnical Commission.
IEE	Institution of Electrical Engineers.
IEEE	Institute of Electrical and Electronic Engineers. A US-based international professional society that issues its own standards and, which is a member of ANSI and ISO.
Illumination Component	An amount of source light incident on the object being viewed.
Impedance	The total opposition that a circuit offers to the flow of alternating current or any other varying current at a particular frequency. It is a combination of resistance R and reactance X, measured in ohms.
Individual Gain per Channel	A system allowing an individual gain level for each input channel, thereby allowing a much wider range of input levels and types without sacrificing accuracy on low-level signals.
Inductance	The property of a circuit or circuit element that opposes a change in current flow, thus causing current changes to lag behind voltage changes. It is measured in henrys.
Insulation Resistance (IR)	That resistance offered by an insulation to an impressed dc voltage, tending to produce a leakage current though the insulation.
Interface	A shared boundary defined by common physical interconnection characteristics, signal characteristics and measuring of interchanged signals.
Interlace	This is the display of two fields alternately with one field filling in the blank lines of the other field so that they interlock. The PAL standard displays 25 video frames per second.
Interlaced	Interlaced - describing the standard television method of raster scanning, in which the image is the product of two fields, each of which is a series of successively scanned lines separated by the equivalent of one line. Thus adjacent lines belong to different fields.
Interrupt	An external event indicating that the CPU should suspend its current task to service a designated activity.
Interrupt Handler	The section of the program that performs the necessary operation to service an interrupt when it occurs.
IP	Internet Protocol.
ISA	Industry Standard Architecture (for IBM Personal Computers).
ISA	Instrument Society of America.
ISB	Intrinsically Safe Barrier.

ISDN	Integrated Services Digital Network. A fairly recent generation of worldwide telecommunications networks that utilize digital techniques for both transmission and switching. It supports both voice and data communications.
ISO	International Standards Organisation.
Isolation	Electrical separation of two circuits. For example, optical isolation allows a high-voltage signal to be transferred to a low-voltage input without electrical interactions.
Isotropic Antenna	A reference antenna that radiates energy in all directions from a point source.
ISR	Interrupt Service Routine. See Interrupt Handler.
ITU	International Telecommunications Union.
Jabber	Garbage that is transmitted when a LAN node fails and then continuously transmits.
Jumper	A wire connecting one or more pins (on the one end of a cable only, for example).
k (kilo)	Typically multiples of a thousand (e.g. 1 kilometer = 1000 meters)
K	In computer terminology, a K is 2^{10}=1024. This distinguishes it from the SI unit k (kilo) which is 1000.
LAN	Local Area Network. A data communications system confined to a limited geographic area typically about 10 kms with moderate to high data rates (100kbps to 50 Mbps). Some type of switching technology is used, but common carrier circuits are not used.
LCD	Liquid Crystal Display. A low power display system used on many laptops and other digital equipment.
LDM	Limited Distance Modem. A signal converter which conditions and boosts a digital signal so that it may be transmitted further than a standard EIA-232 signal.
Leased (or Private) Line	A private telephone line without inter-exchange switching arrangements.
LED	Light Emitting Diode. A semi-conductor light source that emits visible light or infra red radiation.
LF	Line Feed (ASCII Control-J).
Line Driver	A signal converter that conditions a signal to ensure reliable transmission over an extended distance.
Line Turnaround	The reversal of transmission direction from transmitter to receiver or vice versa when a half duplex circuit is used.
Linearity	A relationship where the output is directly proportional to the input.

Link Layer	Layer 2 of the OSI reference model; also known as the data link layer.
Listener	A device on the GPIB bus that receives information from the bus.
LLC	Logical Link Control (IEEE 802.2).
Loaded Line	A telephone line equipped with loading coils to add inductance in order to minimize amplitude distortion.
Long Wire	A horizontal wire antenna that is one wavelength or greater in size.
Loop Resistance	The measured resistance of two conductors forming a circuit.
Loopback	Type of diagnostic test in which the transmitted signal is returned to the sending device after passing through all, or a portion, of a data communication link or network. A loopback test permits the comparison of a returned signal with the transmitted signal.
Low Pass	Generally referring to filters which allow signals below a specified frequency to pass but attenuate a signal above this specified frequency.
Low-Pass Filter	See LPF.
LPF	Low-Pass Filter. A filter processing one transmission band, extending from zero to a specific cutoff frequency.
LSB	Least Significant Byte or Least Significant Bit.
Luminance	The black and white portion of a video signal which supplies brightness and detail for the picture.
LUT	Look-Up Table. This refers to the memory that stores the values for the point processes. Input pixel values are those for the original image whilst the output values are those displayed on the monitor as altered by the chosen point processes.
Lux	SI unit of luminous incidence of illuminance, equal to one lumen per square metre.
Lux-second	SI unit of light exposure.
m	meter. Metric system unit for length.
M	Mega. Metric system prefix for 10^6.
MAC	Media Access Control (IEEE 802).
Manchester Encoding	Digital technique (specified for the IEEE-802.3 Ethernet baseband network standard) in which each bit period is divided into two complementary halves; a negative to positive voltage transition in the middle of the bit period designates a binary "1", whilst a positive to negative transition represents a "0". The encoding technique also allows the receiving device to recover the transmitted clock from the incoming data stream (self clocking).

MAP	Manufacturing Automation Protocol. A suite of network protocols originated by General Motors which follow the seven layers of the OSI model. A reduced implementation is referred to as a mini-MAP.
Mark	This is equivalent to a binary 1.
Mask	A structure covering certain portions of a photo-sensitive medium during photographic processing.
Masking	Setting portions of an image at a constant value, either black or white. Also the process of outlining an image and then matching it to test images.
Master/Slave	Bus access method whereby the right to transmit is assigned to one device only, the Master, and all the other devices, the Slaves may only transmit when requested.
Master Oscillator	The primary oscillator for controlling a transmitter or receiver frequency. The various types are: Variable Frequency Oscillator (VFO); Variable Crystal Oscillator (VXO); Permeability Tuned Oscillator (PTO); Phase Locked Loop (PLL); Linear Master Oscillator (LMO) or frequency synthesizer.
Media Access Unit	Referred to often as MAU. This is the Ethernet transceiver unit situated on the coaxial cable which then connects to the terminal with a drop cable.
Microwave	AC signals having frequencies of 1 GHz or more.
MIPS	Million Instructions per second.
MMS	Manufacturing Message Services. A protocol entity forming part of the application layer. It is intended for use specifically in the manufacturing or process control industry. It enables a supervisory computer to control the operation of a distributed community of computer based devices.
Modem	MODulator - DEModulator. A device used to convert serial digital data from a transmitting terminal to a signal suitable for transmission over a telephone channel or to reconvert the transmitted signal to serial digital data for the receiving terminal.
Modem Eliminator	A device used to connect a local terminal and a computer port in lieu of the pair of modems to which they would ordinarily connect, allow DTE to DTE data and control signal connections otherwise not easily achieved by standard cables or connections.
Modulation Index	The ratio of the frequency deviation of the modulated wave to the frequency of the modulating signal.
Morphology	The study of a structure/form of object in an image.
MOS	Metal Oxide Semiconductor.
MOV	Metal Oxide Varistor.

MSB	Most Significant Byte or Most Significant Bit.
MTBF	Mean Time Between Failures.
MTTR	Mean Time To Repair.
Multidrop	A single communication line or bus used to connect three or more points.
Multiplexer (MUX)	A device used for division of a communication link into two or more channels, either by using frequency division or time division.
Multiplexer	A technique in which multiple signals are combined into one channel. They can then be demultiplexed back into the original components.
NAK	Negative Acknowledge (ASCII Control-U).
Narrowband	A device that can only operate over a narrow band of frequencies.
Negative True Logic	The inversion of the normal logic where the negative state is considered to be TRUE (or 1) and the positive voltage state is considered to be FALSE (or 0).
Network Layer	Layer 3 in the OSI model; the logical network entity that services the transport layer responsible for ensuring that data passed to it from the transport layer is routed and delivered throughout the network.
Network Architecture	A set of design principles including the organisation of functions and the description of data formats and procedures used as the basis for the design and implementation of a network (ISO).
Network	An interconnected group of nodes or stations.
Network Topology	The physical and logical relationship of nodes in a network; the schematic arrangement of the links and nodes of a network typically in the form of a star, ring, tree or bus topology.
NMRR	Normal Mode Rejection Ratio - The ability of a board to filter out noise from external sources, such as AC power lines. NMRR filtering compensates for transient changes in the incoming signal to provide greater accuracy. The higher the NMRR, the better the filtering of incoming data will be.
Node	A point of interconnection to a network.
Noise	A term given to the extraneous electrical signals that may be generated or picked up in a transmission line. If the noise signal is large compared with the data carrying signal, the latter may be corrupted resulting in transmission errors.
Non-linearity	A type of error in which the output from a device does not relate to the input in a linear manner.
NRZ	Non Return to Zero. Pulses in alternating directions for successive 1 bits but no change from existing signal voltage for 0 bits.

NRZI	Non Return to Zero Inverted.
NTSC	National Television System Committee (USA). A television standard specifying 525 lines and 60 fields per second.
Null Modem	A device that connects two DTE devices directly by emulating the physical connections of a DCE device.
Number of Channels	This is the number of input lines a board can sample. Single-ended inputs share the same ground connection, while differential inputs have individual two-wire inputs for each incoming signal, allowing greater accuracy and signal isolation. See also multiplexer.
Nyquist Sampling Theorem	In order to recover all the information about a specified signal it must be sampled at least at twice the maximum frequency component of the specified signal.
OCR	Optical Character Recognition, optical character reader.
ohm	Unit of resistance such that a constant current of one ampere produces a potential difference of one volt across a conductor.
OLUT	Output Look-Up Table.
On-board Memory	Incoming data is stored in on-board memory before being dumped into the PC's memory. On a high-speed board, data is acquired at a much higher rate than can be written into PC memory, so it is stored in the on-board buffer memory.
Optical Isolation	Two networks with no electrical continuity in their connection because an optoelectronic transmitter and receiver has been used.
OR	Outside Radius.
OSI	Open Systems Interconnection. A set of defined protocol layers with a standardized interface which allows equipment from different manufacturers to be connected.
Output	An analog or digital output control type signal from the PC to the external 'real world'.
Overlay	One video signal superimposed on another, as in the case of computer-generated text over a video picture.
Packet	A group of bits (including data and call control signals) transmitted as a whole on a packet switching network. Usually smaller than a transmission block.
PAD	Packet Access Device. An interface between a terminal or computer and a packet switching network.
PAL	Phase Alternating Lines. This is the television standard used in Europe and Australia. The PAL standard is 25 frames per second with 625 lines.

Parallel Transmission	The transmission model where multiple data bits are sent simultaneously over separate parallel lines. Accurate synchronisation is achieved by using a timing (strobe) signal. Parallel transmission is usually unidirectional; an example would be the Centronics interface to a printer.
Parametric Amplifier	An inverting parametric device for amplifying a signal without frequency translation from input to output.
Parasitic	Undesirable electrical parameter in a circuit such as oscillations or capacitance.
Parity Bit	A bit that is set to a "0" or "1" to ensure that the total number of 1 bits in the data and parity fields are even or odd.
Parity Check	The addition of non information bits that make up a transmission block to ensure that the total number of data and parity bits is always even (even parity) or odd (odd parity). Used to detect transmission errors but rapidly losing popularity because of its weakness in detecting errors.
Passive Filter	A circuit using only passive electronic components such as resistors, capacitors and inductors.
Passive Device	Device that must draw its power from connected equipment.
Path Loss	The signal loss between transmitting and receiving antennas.
PBX	Private Branch Exchange.
PCIP	Personal Computer Instrument Products.
PCM	Pulse Code Modulation. The sampling of a signal and encoding the amplitude of each sample into a series of uniform pulses.
PDU	Protocol Data Unit.
PEP	Peak Envelope Power. Maximum amplitude that can be achieved with any combination of signals.
Perigee	The point in an elliptical orbit that is closest to earth.
Peripherals	The input/output and data storage devices attached to a computer e.g. disk drives, printers, keyboards, display, communication boards, etc.
Phase Shift Keying	A modulation technique (also referred to as PSK) used to convert binary data into an analog form comprising a single sinusoidal frequency signal whose phase varies according to the data being transmitted.
Phase Modulation	The sine wave or carrier has its phase changed in accordance with the information to be transmitted.
Physical Layer	Layer 1 of the ISO/OSI Reference Model, concerned with the electrical and mechanical specifications of the network termination equipment.

PIA	Peripheral Interface Adapter. Also referred to as PPI (Programmable Peripheral Interface).
Pixel	One element of a digitized image, sometimes called picture element, or pel.
PLC	Programmable Logic Controller.
PLL	Phase Locked Loop
Point to Point	A connection between only two items of equipment.
Polar Orbit	The path followed when the orbital plane includes the north and south poles.
Polarisation	The direction of an electric field radiated from an antenna.
Polling	A means of controlling I/O devices on a multipoint line in which the CPU queries ('polls') the devices at regular intervals to check for data awaiting transfer (to the CPU). Slower and less efficient than interrupt driven I/O operations.
Polyethylene	A family of insulators derived from the polymerisation of ethylene gas and characterized by outstanding electrical properties, including high IR, low dielectric constant, and low dielectric loss across the frequency spectrum.
Polyvinyl Chloride (PVC)	A general purpose family of insulations whose basic constituent is polyvinyl chloride or its copolymer with vinyl acetate. Plasticisers, stabilizers, pigments and fillers are added to improve mechanical and/ or electrical properties of this material.
Port	A place of access to a device or network, used for input/output of digital and analog signals.
PPI	See PIA.
Presentation Layer	Layer 6 of the ISO/OSI Reference Model, concerned with negotiation of a suitable transfer syntax for use during an application. If this is different from the local syntax, the translation is to/from this syntax.
Pretrigger	Boards with 'pretrigger' capability keep a continuous buffer filled with data, so when the trigger conditions are met, the sample includes the data leading up to the trigger condition.
Profibus	Process Field Bus developed by a consortium of mainly German companies with the aim of standardisation.
Program I/0	The standard method of memory access, where each piece of data is assigned to a variable and stored individually by the PC's processor.

Programmable Gain	Using an amplifier chip on an A/D board, the incoming analog signal is increased by the gain multiplication factor. For example; if the input signal is in the range of -250 mV to +250 mV, the voltage after the amplifier chip set to a gain of 10 would be -2.5 V to +2.5 V.
PROM	Programmable Read Only Memory. This is programmed by the manufacturer as a fixed data or program which cannot easily be changed by the user.
Protocol Entity	The code that controls the operation of a protocol layer.
Protocol	A formal set of conventions governing the formatting, control procedures and relative timing of message exchange between two communicating systems.
PSDN	Public Switched Data Network. Any switching data communications system, such as Telex and public telephone networks, which provides circuit switching to many customers.
PSTN	Public Switched Telephone Network. This is the term used to describe the (analog) public telephone network.
PTT	Post, Telephone and Telecommunications Authority.
Public Switched Network	Any switching communications system - such as Telex and public telephone networks - that provides circuit switching to many customers.
Pulse Input	A square wave input from a real world device such as a flow meter, which sends pulses proportional to the flow rate.
QAM	Quadrature Amplitude Modulation.
QPSK	Quadrature Phase Shift Keying.
Quagi	An antenna consisting of both full wavelength loops (quad) and Yagi elements.
R/W	Read/Write.
RAM	Random Access Memory. Semiconductor read/write volatile memory. Data is lost if the power is turned off.
RAMDAC	Random Access Memory Digital-to-Analog Converter.
Range	The difference between the upper and lower limits of the measured value.
Range Select	The full-scale range a board uses is selected by one of three methods: through the appropriate software, by a hardware jumper on the
board,	or through the use of an external reference voltage.
Raster	The pattern of lines traced by rectilinear scanning in display systems.
Reactance	The opposition offered to the flow of alternating current by inductance or capacitance of a component or circuit.

Real-time	A system is capable of operating in real-time when it is fast enough to react to the real-world events.
Reflectance Component	The amount of light reflected by an object in the scene being viewed.
Refresh rate	The speed at which information is updated on a computer display (CRT).
Repeater	An amplifier which regenerates the signal and thus expands the network.
Resistance	The ratio of voltage to electrical current for a given circuit measured in ohms.
Resolution	The number of bits in which a digitized value will be stored. This represents the number of divisions into which the full-scale range will be divided; for example, a 0-10 V range with a 12-bit resolution will have 4096(2^{12}) divisions of 2.44mV each.
Response Time	The elapsed time between the generation of the last character of a message at a terminal and the receipt of the first character of the reply. It includes terminal delay and network delay.
RF	Radio Frequency.
RFI	Radio Frequency Interference.
RGB	Red/Green/Blue. An RGB signal has four separate elements; red/green/ blue and sync. This results in a cleaner image than with composite signals due to the lower level of distortion and interference.
Ring	Network topology commonly used for interconnection of communities of digital devices distributed over a localized area, e.g. a factory or office block. Each device is connected to its nearest neighbours until all the devices are connected in a closed loop or ring. Data are transmitted in one direction only. As each message circulates around the ring, it is read by each device connected in the ring.
Ringing	An undesirable oscillation or pulsating current.
Rise Time	The time required for a waveform to reach a specified value from some smaller value.
RLE	Run Length Encoder. A digital image method whereby the first grey level of each sequential point-by-point sample and its position in the succession of grey levels is encoded. It is used where there is a tendency for long runs of repeated digitized grey levels to occur.
RMS	Root Mean Square.
ROI	Region of Interest.

ROM	Read Only Memory. Computer memory in which data can be routinely read but written to only once using special means when the ROM is manufactured. A ROM is used for storing data or programs on a permanent basis.
Router	A linking device between network segments which may differ in Layers 1, 2a and 2b of the ISO/OSI Reference Model.
RS	Recommended Standard, for example, RS-232C. More recent designations use EIA, for example, EIA-232C.
RS-232C	Interface between DTE and DCE, employing serial binary data exchange. Typical maximum specifications are 50 feet (15m) at 19200 baud.
RS-422	Interface between DTE and DCE, employing the electrical characteristics of balanced voltage interface circuits.
RS-423	Interface between DTE and DCE, employing the electrical characteristics of unbalanced voltage digital interface circuits.
RS-449	General purpose 37-pin and 9-pin interface for DCE and DTE employing serial binary interchange.
RS-485	The recommended standard of the EIA that specifies the electrical characteristics of drivers and receives for use in balanced digital multipoint systems.
RTU	Remote Terminal Unit. Terminal Unit situated remotely from the main control system.
S-Video	The luminance and chrominance elements of a video signal are isolated from each other, resulting in a far cleaner image with greater resolution.
SAA	Standards Association of Australia.
SAP	Service Access Point.
SDLC	Synchronous Data Link Control. IBM standard protocol superseding the bisynchronous standard.
Selectivity	A measure of the performance of a circuit in distinguishing the desired signal from those at other frequencies.
Self-calibrating	A self-calibrating board has an extremely stable on-board reference which is used to calibrate A/D and D/A circuits for higher accuracy.
Self-diagnostics	On-board diagnostic routine which tests most, if not all, of a board's functions at power-up or on request.
Serial Transmission	The most common transmission mode in which information bits are sent sequentially on a single data channel.
Session Layer	Layer 5 of the ISO/OSI Reference Model, concerned with the establishment of a logical connection between two application entities and with controlling the dialogue (message exchange) between them.

Shielding	The process of protecting an instrument or cable from external noise (or sometimes protecting the surrounding environment of the cable from signals within the cable.)
Short Haul Modem	A signal converter which conditions a digital signal to ensure reliable transmission over DC continuous private line metallic circuits, without interfering with adjacent pairs of wires in the same telephone cables.
Shutter	A mechanical or electronic device used to control the amount of time a light-sensitive material is exposed to radiation.
SI	International metric system of units (Système Internationale).
Sidebands	The frequency components which are generated when a carrier is frequency-modulated.
Upconverter	A device used to translate a modulated signal to a higher band of frequencies.
Sidereal Day	The period of an earth's rotation with respect to the stars.
Signal to Noise Ratio	The ratio of signal strength to the level of noise.
Signal Conditioning	Pre-processing of a signal to bring it up to an acceptable quality level for further processing by a more general purpose analog input system.
Simplex Transmission	Data transmission in one direction only.
Simultaneous Sampling	The ability to acquire and store multiple signals at exactly the same moment. Sample-to-sample inaccuracy is typically measured in nanoseconds.
Single-ended	See number of channels.
Slew Rate	This is defined as the rate at which the voltage changes from one value to another.
Smart Sensors	A transducer (or sensor) with an on-board microprocessor to pre-process input signals to the transducer. It also has the capability of communicating digitally back to a central control station.
SNA	Systems Network Architecture.
SNR	Signal to Noise Ratio.
Software Drivers	Typically a set of programs or subroutines allowing the user to control basic board functions, such as setup and data acquisition. These can be incorporated into user-written programs to create a simple but functional DAS system. Many boards come with drivers supplied.
Software Trigger	Software control of data acquisition triggering. Most boards are designed for software control.
SOH	Start of Header (ASCII Control-A).

Space	Absence of signal. This is equivalent to a binary zero.
Spark Test	A test designed to locate imperfections (usually pin-holes) in the insulation of a wire or cable by application of a voltage for a very short period of time while the wire is being drawn through the electrode field.
Spatial Resolution	A measure of the level of detail a vision system can display. The value, expressed in mils or inches per pixel, is derived by dividing the linear dimensions of the field of view (x and y, as measured in the image plane), by the number of pixels in the x and y dimensions of the system's imaging array or image digitizer.
Spatial Filtering	In image processing, the enhancement of an image by increasing or decreasing its spatial frequencies.
Spectral Purity	The relative quality of a signal measured by the absence of harmonics, spurious signals and noise.
Speed/Typical Throughput	The maximum rate at which the board can sample and convert incoming samples. The typical throughput is divided by the number of channels being sampled to arrive at the samples/second on each channel. To avoid false readings, the samples per second on each channel need to be greater than twice the frequency of the analog signal being measured.
Standing Wave Ratio	The ratio of the maximum to minimum voltage (or current) on a transmission line at least a quarter-wavelength long. (VSWR refers to voltage standing wave ratio)
Star	A type of network topology in which there is a central node that performs all switching (and hence routing) functions.
Statistical Multiplexer	Multiplexer in which data loading from multiple devices occurs randomly throughout time, in contrast to standard multiplexers where data loading occurs at regular predictable intervals.
STP	Shielded Twisted Pair.
Straight Through Pinning	EIA-232 and EIA-422 configuration that match DTE to DCE, pin for pin (pin 1 with pin 1, pin 2 with pin 2,etc).
Strobe	A handshaking line used to signal to a receiving device that there is data to be read.
STX	Start of Text (ASCII Control-B).
Subharmonic	A frequency that is a integral submultiple of a reference frequency.
Switched Line	A communication link for which the physical path may vary with each use, such as the public telephone network.
Sync	A synchronisation, or sync, pulse ensures that the monitor displaying the information is synchronized at regular intervals with

	the device supplying the data, thus displaying the data at the right location.
	For example, a sync pulse would be used between a camera and a display device to reset the image to the top of the frame for the beginning of the image.
Synchronisation	The co-ordination of the activities of several circuit elements.
Synchronous Transmission	Transmission in which data bits are sent at a fixed rate, with the transmitter and receiver synchronized. Synchronized transmission eliminates the need for start and stop bits.
Talker	A device on the GPIB bus that simply sends information onto the bus without actually controlling the bus.
Tank	A circuit comprising inductance and capacitance which can store electrical energy over a finite band of frequencies.
TCP/IP	Transmission Control Protocol/Internet Protocol. The collective term for the suite of layered protocols that ensures reliable data transmission in an internet (a network of packet switching networks functioning as a single large network).
	Originally developed by the US Department of Defense in an effort to create a network that could withstand an enemy attack.
TDM	Time Division Multiplexer. A device that accepts multiple channels on a single transmission line by connecting terminals, one at a time, at regular intervals, interleaving bits (bit TDM) or characters (Character TDM) from each terminal.
TDR	Time Domain Reflectometer. This testing device sends pulses down the cable and enables the user to determine cable quality (distance to defect and type of defect) by the reflections received back.
Temperature Rating	The maximum, and minimum temperature at which an insulating material may be used in continuous operation without loss of its basic properties.
Text Mode	Signals from the hardware to the display device are only interpreted as text characters.
Thresholding	The process of defining a specific intensity level for determining which of two values will be assigned to each pixel in binary processing. If the pixel's brightness is above the threshold level, it will appear in white in the image; if it is below the threshold level, it will appear black.
TIA	Telecommunications Industry Association.
Time Division	The process of transmitting multiple signals over a single channel by multiplexing taking samples of each signal in a repetitive time sequenced fashion.

Time Sharing	A method of computer operation that allows several interactive terminals to use one computer.
Time Domain	The display of electrical quantities versus time.
Token Ring	Collision free, deterministic bus access method as per IEEE 802.2 ring topology.
TOP	Technical Office Protocol. A user association in USA which is primarily concerned with open communications in offices.
Topology	Physical configuration of network nodes, e.g. bus, ring, star, tree.
Transceiver	A combination of transmitter and receiver.
Transducer	Any device that generates an electrical signal from real-world physical measurements. Examples are LVDTs, strain gauges, thermocouples and RTDs. A generic term for sensors and their supporting circuitry.
Transient	An abrupt change in voltage of short duration.
Transmission Line	One or more conductors used to convey electrical energy from one point to another.
Transport Layer	Layer 4 of the ISO/OSI Reference Model, concerned with providing a network independent reliable message interchange service to the application oriented layers (layers 5 through 7).
Trigger	A rising edge at an 8254 timer/counter's gate input.
Trunk	A single circuit between two points, both of which are switching centres or individual distribution points. A trunk usually handles many channels simultaneously.
Twisted Pair	A data transmission medium, consisting of two insulated copper wires twisted together. This improves its immunity to interference from nearby electrical sources that may corrupt the transmitted signal.
UART	Universal Asynchronous Receiver/Transmitter. An electronic circuit that translates the data format between a parallel representation, within a computer, and the serial method of transmitting data over a communications line.
UHF	Ultra High Frequency.
Unbalanced Circuit	A transmission line in which voltages on the two conductors are unequal with respect to ground e.g. a coaxial cable.
Unipolar Inputs	When set to accept a unipolar signal, the channel detects and converts only positive voltages. (Example: 0 to +10 V).
Unloaded Line	A line with no loaded coils that reduce line loss at audio frequencies.
Upconverter	A device used to translate a modulated signal to a higher band of frequencies.
Uplink	The path from an earth station to a satellite.

USRT	Universal Synchronous Receiver/Transmitter. See UART.
UTP	Unshielded Twisted Pair.
V.35	CCITT standard governing the transmission at 48 kbps over 60 to 108 kHz group band circuits.
VCO	Voltage controlled oscillator. Uses variable DC applied to tuning diodes to change their junction capacitances. This results in the output frequency being dependent on the input voltage.
Velocity of Propagation	The speed of an electrical signal down a length of cable compared to speed in free space expressed as a percentage.
VFD	Virtual Field Device. A software image of a field device describing the objects supplied by it eg measured data, events, status etc which can be accessed by another node on the network.
VGA	Video Graphics Array. This standard utilizes analog signals only (between 0 and 1 V) offering a resolution of 640 by 480 pixels, a palette of 256 colors out of 256000 colors and the ability to display 16 colors at the same time.
VHF	Very High Frequency.
Vidicon	A small television tube originally developed for closed-circuit television. It is about one inch (2.54 cm) in diameter and five inches (12.7 cm) long. Its controls are relatively simple and can be operated by unskilled personnel. The Vidicon is widely used in broadcast service.
Volatile Memory	A storage medium that loses all data when power is removed.
Voltage Rating	The highest voltage that may be continuously applied to a wire in conformance with standards of specifications.
VRAM	Volatile Random Access Memory. See RAM.
VSD	Variable Speed Drive.
VT	Virtual Terminal.
WAN	Wide Area Network.
Waveguide	A hollow conducting tube used to convey microwave energy.
Wedge Filter	An optical filter so constructed that the density increases progressively from one end to the other, or angularly around a circular disk.
Word	The standard number of bits that a processor or memory manipulates at one time. Typically, a word has 16 bits.
X.21	CCITT standard governing interface between DTE and DCE devices for synchronous operation on public data networks.
X.25 Pad	A device that permits communication between non X.25 devices and the devices in an X.25 network.

X.25	CCITT standard governing interface between DTE and DCE device for terminals operating in the packet mode on public data networks.
X.3/X.28/X.29	A set of internationally agreed standard protocols defined to allow a character oriented device, such as a visual display terminal, to be connected to a packet switched data network.
X-ON/X-OFF	Control characters used for flow control, instructing a terminal to start transmission (X-ON) and end transmission (X-OFF).

Appendix B
Units and Abbreviations

Unit Symbol	***Unit***	***Quantity***
m	metre	length
kg	kilogram	mass
s	second	time
A	ampere	electric current
K	kelvin	thermodynamic temp
cd	candela	luminous intensity

Table A.1
SI units

Symbol	***Prefix***	***Factor by which unit is multiplied***
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
h	hecto	10^{2}
da	deca	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
u	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}

Table A.2
Decimal Prefixes

Quantity	Unit	Symbol	Equivalent
plane angle	radian	rad	-
force	newton	N	kg m/s^2
work, energy heat	joule	J	N m
power	watt	W	J/s
frequency	hertz	Hz	s-1
viscosity: kinematic	-	m^2/s	10 c St (Centistoke)
dynamic	-	Ns/m^2 or Pa s	10^3 cP (Centipoise)
pressure	-	Pa or N/m^2	pascal, Pa

Table A.3
Supplementary and Derived Units

Quantity	Electrical unit	Symbol	Derived unit
potential	volt	V	W/A
resistance	ohm	Ω	V/A
charge	coulomb	C	A s
capacitance	farad	F	A s/V
electric field strength	-	V/m	-
electric flux density	-	C/m^2	-

Table A.4
Supplementary and Derived Unit (electrical)

Quantity	Magnetic unit	Symbol	Derived unit
magnetic flux	weber	Wb	V s = Nm/A
inductance	henry	H	V s/A = Nm/A^2
magnetic field strength	-	A/m	-
magnetic flux density	tesla	T	Wb/m^2 = (N)/(Am)

Table A.5
Supplementary and Derived Units (magnetic)

Name	***Symbol***	***Equivalent***
Avogadro's number	N	6.023×10^{26} /(kg mol)
Bohr magneton	B	9.27×10^{-24} A m 25^2
Boltzmann's constant	k	1.380×10^{-23} J/k
Stefan-Boltzmann constant	d	5.67×10^{-8} W/(m^2K^4)
Characteristic impedance of free space	Z_o	$(\mu_o/E_o)^{1/2}=120\pi\Omega$
Electron volt	eV	1.602×10^{-19}J
Electron charge	e	1.602×10^{-19}C
Electronic rest mass	m_e	9.109×10^{-31}kg
Electronic charge to mass ratio	e/m_e	1.759×10^{11} C/kg
Faraday constant	F	9.65×10^{7} C/(kg mol)
Permeability of free space	μ_o	$4\pi \times 10^{-7}$ H/m
Permittivity of free space	E_o	8.85×10^{-12} F/m
Planck's constant	h	6.626×10^{-34} J s
Proton mass	m_p	1.672×10^{-27} kg
Proton to electron mass ratio	m_p/m_e	1835.6
Standard gravitational acceleration	g	9.80665 m/s^2 9.80665 N/kg
Universal constant of gravitation	G	6.67×10^{-11} N m^2/kg^2
Universal gas constant	R_o	8.314 kJ/(kg mol K)
Velocity of light in vacuo	C	2.9979×10^{8} m/s
Volume of 1 kg mol of ideal gas at 1 atm & 0^oC	-	22.41 m^3
Temperature	^0C	$5/9(^0F - 32)$
Temperature	K	$5/9(^0F + 459.67)$ $5/9^0R$ $^0C + 273.15$

Table A.6
Physical Constants

Appendix C
Commonly used Formulae

Symbols used in formulae

The symbols described in the following table are used in the formulae shown in the next section

Symbol	*Description*	*SI Unit*
a	Velocity of sound	ms^{-1}
a	Acceleration	ms^{-2}
A	Area	m^2
c	Velocity of light	ms^{-1}
C	Capacitance	F
D	Diameter	m
E	Young's modulus	Nm^{-2}
ΔE	Energy difference	J
f	Frequency	Hz
F	Force	N
H	Magnetising force magnetic field strength	Am^{-1}
I	Current	A
I	Moment of inertia	kgm^2
k	Radius of gyration	m
kp	Pitch factor of winding	-
l	Length	m
l	Length of conductor	m
L	Inductance	H
m	Mass	kg
M	Momentum	$kg.m.s^{-1}$
n	Speed of rotation	rpm
N	Number of turns	-
p	Number of pole pairs	-

Symbol	***Description***	***SI Unit***
Q	Volumetric flow rate	m^3s^{-1}
Q	Charge	C
R	Resistance	Ω
s	Fractional slip	-
t	Time	s
T	Time Factor	-
T	Torque	Nm
T	Temperature (absolute)	K
ΔT	Temperature difference	°C
u	Velocity	ms^{-1}
v	Velocity	ms^{-1}
V	Voltage	V
V	Volume	m^3
x	Distance (variables as in dx)	m
Z	Number of armature conductors	-
Z	Impedance	Ω
a	Coefficient of volumetric expansion	Hm/(mK)
a	Resistance coefficient	$\Omega\ K^{-1}$
b	Coefficient of volumetric expansion	K^{-1}
e_o	Permittivity of free space	Fm^{-1}
e_o	Permittivity-relative	-
m_o	Permeability of free space	Hm^{-1}
m_r	Permeability-relative	-
r_o	Resistivity	$\Omega\ m^3$
r	Density	kgm^3
s	Stefan-Boltzmann constant	$Wm^{-2}K^{-4}$
φ	Angle	radians
F	Magnetic flux, flux per pole	Wb
w	Angular Velocity	$rad.s^{-1}$
w_n	Natural frequency	$rad.s^{-1}$
w_o	Natural frequency	$rad.s^{-1}$
w_d	Damped natural frequency	$rad.s^{-1}$

Formulae

Ohm's Law (DC version)

$$V = IR$$

$$I = \frac{V}{R}$$

Ohm's Law (AC version)

$$\underline{V} = \underline{I} \cdot \underline{Z}$$

Kirchhoff's Law

$$\sum_{j=0}^{N} I_j = 0$$

Power

$$P_{dc} = VI = I^2 R = \frac{V^2}{R}$$

$$P_{ac} = \mathrm{Re}(\underline{V} \cdot \underline{I}) = VI\cos\phi$$

Resistance

Resistors in series:

$$R = R_1 + R_2 + R_3 + \ldots$$

Resistors in parallel:

$$R = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \ldots}$$

Inductance

$$V = -L\frac{dI}{dt}$$

$$I = -\int \frac{V}{L} dt$$

$$L = N^2 \mu_O \mu_r \frac{a}{l}$$

for LR circuit decay, stored energy is calculated as follows:

$$Energy = \frac{1}{2} L I^2$$

Capacitance

$$Q = CV = \int idt$$

$$i = \frac{dQ}{dt} = C\frac{dV}{dt}$$

For n parallel plates:

$$C = \varepsilon_o \varepsilon_r (n-1)\frac{a}{d}$$

$$\varepsilon_o = 8.85x10^{-12} Fm^{-1}$$

For RC circuit discharge:

$$i = -Ie^{-\frac{1}{RC}}$$

Stored energy:

$$i = \frac{1}{2}\varepsilon_o \varepsilon_r a\left(\frac{V}{x}\right)^2$$

For capacitors in series:

$$C_{total} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \ldots}$$

For capacitors in parallel:

$$C_{total} = C_1 + C_2 + C_3 + \ldots$$

Electrostatics

$$F = \frac{Q_1 Q_2}{4\pi\varepsilon_0 r^2}$$

$$\underline{F} = e \cdot \underline{E} = -e\Delta V$$

$$\underline{D} = e_o e_r \underline{E}$$

Electromagnetism

$$E = -N\frac{d\phi}{dt}$$

$$B = \mu_o \frac{1}{2\pi r}$$

$$F = BlI$$

$$F = \mu_o I_1 I_2 \frac{1}{2\pi d}$$

$$\frac{dH}{dl} = \frac{I \sin\alpha}{4\pi x^2}$$

For a solenoid:

$$H = \frac{NI}{l}$$

Magnetism

$$H = \frac{B}{\mu_o \mu_r}$$

For a magnetic circuit:

$$B = \frac{\varphi}{a}$$

Stored energy density:

$$Energy = \frac{1}{2} HB = \frac{1}{2} \frac{B^2}{\mu_o}$$

AC Circuits

$$V_{max} = \frac{1}{\sqrt{2}} V_{peak}$$

$$\text{abs}(Z) = \left\{ R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2 \right\}^{1/2}$$

$$Z = R + j\omega L + \frac{1}{j\omega C}$$

$$\text{Cos}\ \phi = \frac{R}{Z}$$

At resonance the following relationship holds true:

$$w = w_o = \frac{1}{\sqrt{LC}}$$

The Q factor can be calculated as follows:

$$Q_{factor} = w_o \frac{L}{R}$$

Sound

Note that decibels are not units as such but a ratio of voltages, currents and power, for example:

$$dB = 10 \log_{10} \frac{P_1}{P_2}$$

where: P_1, P_2 are the power levels:

$$dB = 20 \log_{10} \frac{V_1}{V_2}$$

For differing input and output impedances the following formula is appropriate:

$$dB = 20\,Log_{10} \frac{V_1}{V_2} \quad + \quad 10\,Log_{10} \frac{Z_2}{Z_1}$$

Where V_1, V_2 are the voltages
Z_1, Z_2 are the impedances.

Appendix D
Resistor Color Coding

Resistor values are calculated according to the following color coding:

Color on resistor	*Value allocation*
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Voilet/Purple	7
Grey	8
White	9

Table D.1

Common Band Colors

Resistors have the following two major groupings of color coding:

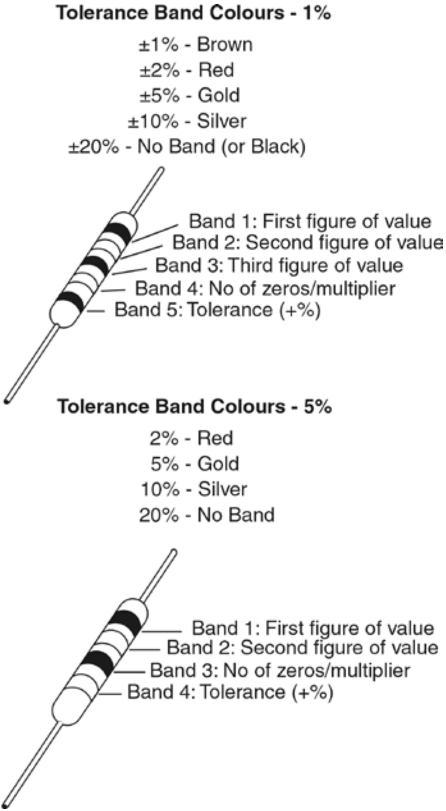


Figure D.1
Color coding for tolerance resistors

Appendix E
Binary Encoding of Quantization Levels

Consider an n-bit binary number representing a full scale range R. In other words, the range R is being quantized into 2^n quantization levels. If R is unipolar, the quantized value x_Q lies in the range [0,R). If it is bipolar, x_Q lies in the range [-R/2,R/2).

We shall denote the n bit pattern as a vector $b = [b_{n-1}, b_{n-2}, \ldots, b_1, b_0]$ where b_{n-1} is called the most significant bit (MSB) and b_0 is the least significant bit (LSB). There are many ways in which this n bit pattern can be used to encode x_Q.

Three most common ways are:

1. Unipolar natural binary

$$x_Q = R(b_{n-1}2^{-1} + b_{n-2}2^{-2} + \quad + b_1 2^{-(n-1)} + b_0 2^{-n})$$

2. Bipolar offset binary

$$x_Q = R(b_{n-1}2^{-1} + b_{n-2}2^{-2} + \quad + b_1 2^{-(n-1)} + b_0 2^{-n} - 0.5)$$

3. Bipolar two's complement

$$x_Q = R(b_{n-1}2^{-1} + b_{n-2}2^{-2} + \quad + b_1 2^{-(n-1)} + b_0 2^{-n} - 0.5)$$

Here b_{n-1} denotes the complement of bn-1.

See example overleaf.

Example

For R=2 V and 3-bit (8-level) quantization, the correspondence between the binary representations and the quantized value are given in the following table.

$b_2b_1b_0$	Natural Binary	Offset Binary	2's Complement
111	1.75	0.75	-0.25
110	1.50	0.50	-0.50
101	1.25	0.25	-0.75
100	1.00	0.00	-1.00
011	0.75	-0.25	0.75
010	0.50	-0.50	0.50
001	0.25	-0.75	0.25
000	0.00	-1.00	0.00

Table E1
Example

The unipolar natural binary representation encodes levels in the range 0 to 2V. Offset binary and 2's complement encodes –1V to 1V.

Who is IDC Technologies

IDC Technologies is a specialist in the field of industrial communications, telecommunications, automation and control and has been providing high quality training on an international basis for more than 16 years.

IDC Technologies consists of an enthusiastic team of professional engineers and support staff who are committed to providing the highest quality in their consulting and training services.

The Benefits to You of Technical Training

The technological world today presents tremendous challenges to engineers, scientists and technicians in keeping up to date and taking advantage of the latest developments in the key technology areas.

The immediate benefits of attending an IDC Technologies workshop are:

- Gain practical hands-on experience
- Enhance your expertise and credibility
- Save $$$ for your company
- Obtain state of the art knowledge for your company
- Learn new approaches to troubleshooting
- Improve your future career prospects

The IDC Technologies Approach to Training

All workshops have been carefully structured to ensure that attendees gain maximum benefits. A combination of carefully designed training software, hardware and well written documentation, together with multimedia techniques ensure that the workshops are presented in an interesting, stimulating and logical fashion.

IDC Technologies has structured a number of workshops to cover the major areas of technology. These courses are presented by instructors who are experts in their fields, and have been attended by thousands of engineers, technicians and scientists world-wide, who have given excellent reviews.

The IDC Technologies team of professional engineers is constantly reviewing the courses and talking to industry leaders in these fields, thus keeping the workshops topical and up to date.

Technical Training Workshops

IDC is continually developing high quality state of the art workshops aimed at assisting engineers, technicians and scientists. Current workshops include:

DATA COMMUNICATIONS & NETWORKING

- Best Practice in Industrial Data Communications
- Practical Data Communications & Networking for Engineers and Technicians
- Practical DNP3, 60870.5 & Modern SCADA Communication Systems
- Practical Troubleshooting & Problem Solving of Ethernet Networks
- Practical FieldBus and Device Networks for Engineers and Technicians
- Practical Fieldbus, DeviceNet and Ethernet for Industry
- Practical Use and Understanding of Foundation FieldBus for Engineers and Technicians
- Practical Fibre Optics for Engineers and Technicians
- Practical Industrial Communication Protocols
- Practical Troubleshooting & Problem Solving of Industrial Data Communications
- Practical Troubleshooting, Design & Selection of Industrial Fibre Optic Systems for Industry
- Practical Industrial Networking for Engineers & Technicians
- Practical Industrial Ethernet & TCP/IP Networks
- Practical Local Area Networks for Engineers and Technicians
- Practical Routers & Switches (including TCP/IP and Ethernet) for Engineers & Technicians
- Practical TCP/IP and Ethernet Networking for Industry
- Practical Fundamentals of Telecommunications and Wireless Communications
- Practical Radio & Telemetry Systems for Industry
- Practical TCP/IP Troubleshooting & Problem Solving for Industry
- Practical Troubleshooting of TCP/IP Networks
- Practical Fundamentals of Voice over IP (VOIP) for Engineers and Technicians
- Wireless Networking and Radio Telemetry Systems for Industry
- Wireless Networking Technologies for Industry

ELECTRICAL

- Practical Maintenance & Troubleshooting of Battery Power Supplies
- Practical Electrical Network Automation & Communication Systems
- Safe Operation & Maintenance of Circuit Breakers and Switchgear
- Troubleshooting, Maintenance & Protection of AC Electrical Motors and Drives
- Practical Troubleshooting of Electrical Equipment and Control Circuits
- Practical Earthing, Bonding, Lightning & Surge Protection
- Practical Distribution & Substation Automation for Electrical Power Systems
- Practical Solutions to Harmonics in Power Distribution
- Practical High Voltage Safety Operating Procedures for Engineers and Technicians

- Practical Electrical Wiring Standards - National Rules for Electrical Installations -
- Lightning, Surge Protection and Earthing of Electrical & Electronic Systems
- Practical Power Distribution
- Practical Power Quality: Problems & Solutions

ELECTRONICS

- Practical Digital Signal Processing Systems for Engineers and Technicians
- Practical Embedded Controllers: Troubleshooting and Design
- Practical EMC and EMI Control for Engineers and Technicians
- Practical Industrial Electronics for Engineers and Technicians
- Practical Image Processing and Applications
- Power Electronics and Variable Speed Drives: Troubleshooting & Maintenance
- Practical Shielding, EMC/EMI, Noise Reduction, Earthing and Circuit Board Layout

INFORMATION TECHNOLOGY

- Practical Web-Site Development & E-Commerce Systems for Industry
- Industrial Network Security for SCADA, Automation, Process Control & PLC Systems
- SNMP Network Management: The Essentials
- VisualBasic Programming for Industrial Automation, Process Control & SCADA Systems

INSTRUMENTATION, AUTOMATION & PROCESS CONTROL

- Practical Analytical Instrumentation in On-Line Applications
- Practical Alarm Systems Management for Engineers and Technicians
- Practical Programmable Logic Controller's (PLCs) for Automation and Process Control
- Practical Batch Management & Control (Including S88) for Industry
- Practical Boiler Control and Instrumentation for Engineers and Technicians
- Practical Programming for Industrial Control - using (IEC 1131-3 and OPC)
- Practical Distributed Control Systems (DCS) for Engineers & Technicians
- Practical Data Acquisition using Personal Computers and Standalone Systems
- Best Practice in Process, Electrical & Instrumentation Drawings and Documentation
- Practical Troubleshooting of Data Acquisition & SCADA Systems
- Practical Industrial Flow Measurement for Engineers and Technicians
- Practical Hazops, Trips and Alarms
- Practical Hazardous Areas for Engineers and Technicians
- A Practical Mini MBA in Instrumentation and Automation
- Practical Instrumentation for Automation and Process Control
- Practical Intrinsic Safety for Engineers and Technicians
- Practical Tuning of Industrial Control Loops
- Practical Motion Control for Engineers and Technicians
- Practical SCADA and Automation for Managers, Sales and Admininistration
- Practical Automation, SCADA and Communication Systems: A Primer for Managers

- Practical Fundamentals of OPC (OLE for Process Control)
- Practical Process Control for Engineers and Technicians
- Practical Process Control & Tuning of Industrial Control Loops
- Practical Industrial Programming using 61131-3 for PLCs
- Practical SCADA & Telemetry Systems for Industry
- Practical Shutdown & Turnaround Management for Engineers and Managers
- Practical Safety Instrumentation and Shut-down Systems for Industry
- Practical Fundamentals of E-Manufacturing, MES and Supply Chain Management
- Practical Safety Instrumentation & Emergency Shutdown Systems for Process Industries
- Control Valve Sizing, Selection and Maintenance

MECHANICAL ENGINEERING

- Practical Fundamentals of Heating, Ventilation & Airconditioning (HVAC)
- Practical Boiler Plant Operation and Management for Engineers and Technicians
- Practical Bulk Materials Handling (Conveyors, Bins, Hoppers & Feeders)
- Practical Pumps and Compressors: Control, Operation, Maintenance & Troubleshooting
- Practical Cleanroom Technology and Facilities for Engineers and Technicians
- Gas Turbines: Troubleshooting, Maintenance & Inspection
- Practical Hydraulic Systems: Operation and Troubleshooting
- Practical Lubrication Engineering for Engineers and Technicians
- Practical Safe Lifting Practice and Maintenance
- Practical Mechanical Drives (Belts, Chains etc) for Engineers & Technicians
- Fundamentals of Mechanical Engineering
- Practical Pneumatics: Operations and Troubleshooting for Engineers & Technicians
- Practical Centrifugal Pumps - Optimising Performance
- Practical Machinery and Automation Safety for Industry
- Practical Machinery Vibration Analysis and Predictive Maintenance

PROJECT & FINANCIAL MANAGEMENT

- Practical Financial Fundamentals and Project Investment Decision Making
- How to Manage Consultants
- Marketing for Engineers and Technical Personnel
- Practical Project Management for Engineers and Technicians
- Practical Specification and Technical Writing for Engineers

CHEMICAL ENGINEERING

- Practical Fundamentals of Chemical Engineering

CIVIL ENGINEERING

- Hazardous Waste Management and Pollution Prevention
- Structural Design for non-structural Engineers
- Best Practice in Sewage and Effluent Treatment Technologies

Comprehensive Training Materials

Workshop Documentation

All IDC Technologies workshops are fully documented with complete reference materials including comprehensive manuals and practical reference guides.

Software

Relevant software is supplied with most workshops. The software consists of demonstration programs which illustrate the basic theory as well as the more difficult concepts of the workshop.

Hands-On Approach to Training

IDC Technologies engineers have developed the workshops based on the practical consulting expertise that has been built up over the years in various specialist areas. The objective of training today is to gain knowledge and experience in the latest developments in technology through cost effective methods.

The investment in training made by companies and individuals is growing each year as the need to keep topical and up to date in the industry which they are operating is recognized. As a result, IDC Technologies instructors place particular emphasis on the practical, hands-on aspect of the workshops presented.

On-site Workshops

In addition to the external workshops which IDC Technologies presents on a world-wide basis, all IDC Technologies courses are also available for on-site (in-house) presentation at our clients premises.

On-site training is a cost effective method of training for companies with many delegates to train in a particular area. Organizations can save valuable training $$$ by holding courses on-site, where costs are significantly less. Other benefits are IDC Technologies ability to focus on particular systems and equipment so that attendees obtain only the greatest benefits from the training.

All on-site workshops are tailored to meet with clients training requirements and courses can be presented at beginners, intermediate or advanced levels based on the knowledge and experience of delegates in attendance. Specific areas of interest to the client can also be covered in more detail.

Our external workshops are planned well in advance and you should contact us as early as possible if you require on-site/customized training. While we will always endeavor to meet your timetable preferences, two to three months notice is preferable in order to successfully fulfil your requirements.

Please don't hesitate to contact us if you would like to discuss your training needs.

Customized Training

In addition to standard on-site training, IDC Technologies specializes in customized courses to meet client training specifications. IDC Technologies has the necessary engineering and training expertise and resources to work closely with clients in preparing and presenting specialized courses.

These courses may comprise a combination of all IDC Technologies courses along with additional topics and subjects that are required. The benefits to companies in using training is reflected in the increased efficiency of their operations and equipment.

Training Contracts

IDC Technologies also specializes in establishing training contracts with companies who require ongoing training for their employees. These contracts can be established over a given period of time and special fees are negotiated with clients based on their requirements. Where possible IDC Technologies will also adapt courses to satisfy your training budget.

References from various international companies to whom IDC Technologies is contracted to provide on-going technical training are available on request.

Some of the thousands of Companies world-wide that have supported and benefited from IDC Technologies workshops are:

Australia

Alcoa • Alinta Gas • Ampol Refineries • Ansto • Australian Communications Authority • Australian Geological Society • BHP Billiton • BOC Gases • Boeing Constructors Inc • Brisbane City Council • British Aerospace Australia • Ci Technologies • Civil Aviation Authority • Comalco Aluminium • CSIRO • Delta Electricity • Dept of Defence • Dept of Transport and Works • DSTO • Duke Energy International • Emerson Process Management • Energex • ERG Group • Ergon Energy • ETSA • Gippsland Water • Gladstone Tafe College • Gosford City Council • Great Southern Energy • Hamersley Iron • Hewlett Packard • Holden Ltd • Honeywell • I&E Systems Pty Ltd • Integral Energy • Metro Brick • Millenium Chemicals • Mt Isa Mines • Murdoch University • Nabalco • NEC • Nilson Electric • Normandy Gold • Nu-Lec Industries • Parker Hannafin • Pharmacia & Upjohn • Power & Water Authority NT• Powercor • Powerlink • Prospect Electricity • Queensland Alumina • Raaf • Raytheon • RGC Mineral Sands • Robe River Iron Associates • Royal Darwin Hospital • Santos Ltd • Schneider Electric • Shell • Snowy Mountain Hydro • SPC Fruit • Stanwell Power Station • Telstra • Tiwest • Uncle Bens • Vision • Wesfarmers CSBP • Western Power • Westrail • WMC • Woodside • Worsley Alumina • Wyong Shire • Yokogawa Australia

Botswana

De Beers - Jwaneng Mine • De Beers - Orapa Mine

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Nambia

Namibian Broadcasting Corporation • Nampower • Namwater

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ACI Packaging • Anchor Products • Auckland Regional Council • Ballance Agri Nutrients • Contact Energy • Ericcson • Fisher & Paykel • GEC Alsthom • James Hardie • Methanex • Natural Gas • NZ Water and Waste Assoc • Norske Skog • NZ Aluminium Smelters • NZ Refining Co • Pan Pac Forest Products • Powerco • Rockwell • Rotorua District Council • Royal New Zealand Navy • The University of Auckland

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Activemedia Innovation Pte Ltd • Flotech Controls • Land Transport Authority • Ngee Ann Polytechnic • Power Seraya Ltd • Westinghouse • Yokogawa Singapore

South Africa

Anglo American • Bateman Metals • Caltex Refineries • Chevron • Columbus Stainless • De Beers • Durban Metro • Eastern Cape Tech • Eskom • Grintek Ewation • Highveld Steel • Illovo Sugar • Impala Platinums • Iscor • IST• Joy Mining • Lever Ponds • Metso Automation • Middleburg Ferrochrome • Mintek • Mondi Kraft • Mossgas • Namaqua Sands • Nestle • Orbicom • Rand Water Board • Richards Bay Minerals • SA Navy • SABC • Saldanha Steel • Sappi • Sasol • Spoornet • Umgeni Water • Western Platinum • Witwatersrand Technikon • Yelland Controls

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USA

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IDC Technologies - Worldwide Offices

For further information about current or future workshops please contact your local office:

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